Low-Power IEEE 802.15.4/proprietary FSK Zero-IF 2.4GHz Transceiver IC

Preliminary Technical Data

ADF7242

FEATURES

Frequency range (global ISM band)
- 2400MHz to 2483.5MHz

Programmable data rates and modulation
- IEEE 802.15.4 compatible (250 kbps)
- 62.5 kbps to 2000 kbps FSK/GFSK

Low power consumption
- 18 mA (typ.) in receive mode
- 22 mA (typ.) in transmit mode (Po = 3 dBm)
- 1.25μA 32kHz xtal oscillator wake-up mode

High Sensitivity
- -97 dBm at 250 kbps (IEEE 802.15.4)
- -93 dBm at 250 kbps (GFSK)
- -84 dBm at 2 Mbps (GFSK)

Programmable output power
- -21 dBm to +5 dBm in 2dB steps

Integrated voltage regulator
- 1.8 V to 3.6 V input voltage range

Excellent receiver selectivity and blocking resilience
- Zero-IF architecture
- Complies with EN300 440 class 2, FCC CFR47 part 15, ARIB STD-T66
- Digital RSSI measurement

On-chip packet handling
- 256 bytes for TX /RX Buffer

Flexible multiple RF Port interface

External PA/LNA support hardware

Switched antenna diversity support

Wake up timer

Very few external components
- Integrated PLL loop filter
- No RX/TX switch needed
- Integrated battery monitor
- Temperature sensor
- Integrated RC and 32kHz crystal oscillator

Flexible SPI control interface with burst-mode register access

Small form factor 5x5 mm 32-pin LFCSP package

APPLICATIONS

Wireless sensor networks

Automatic meter reading/Smart metering

Industrial wireless control

Wireless audio / video

Consumer Electronics

Zigbee

FUNCTIONAL BLOCK DIAGRAM

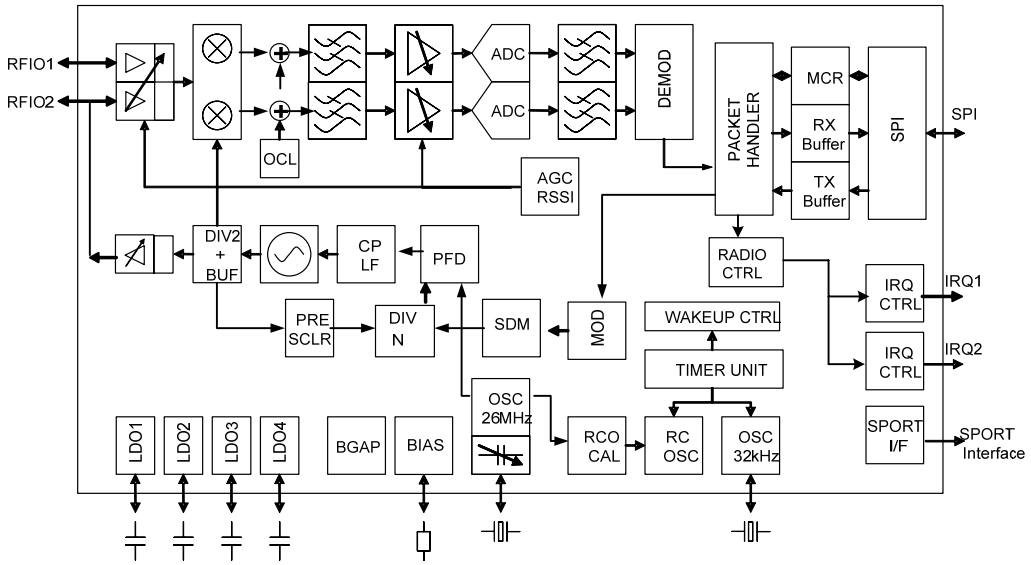

Figure 1

Rev. PrG

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ABBREVIATIONS

ACK	IEEE802.15.4 acknowledgement frame
ADC	Analog to digital converter
AFC	Automatic frequency correction
AGC	Automatic gain control
Battmon	Battery Monitor
BBRAM	Back up battery random access memory
CRC	Cyclic redundancy check
CSMA-CA	Carrier-Sense-Multiple-Access with Collision Avoidance
DR	Data rate
DSSS	Direct sequence spread spectrum
FCS	Frame check sequence
FHSS	Frequency hoping spread spectrum
FSK	Frequency shift keying
GFSK	Gaussian frequency shift keying
LQI	Link quality indicator
MCR	Modem Configuration Register
MER	Modulation Error Ratio
MSK	Minimum shift keying
NC	Not connected
OCL	Offset correction loop
OQPSK	Offset-quadrature phase shift keying
PA	Power amplifier
PHR	PHY Header
PHY	Physical Layer
POR	Power-On Reset
PSDU	PHY service data unit
RC	Radio Controller
RCO32K	32 kHz RC oscillator
RSSI	Receive signal strength indicator
RTC	Real time Clock
Rx	Receive
SFD	Start-of-frame delimiter
Tx	Transmit
VCO	Voltage controlled oscillator
WUC	Wake up controller
XTO26M	26 MHz Crystal oscillator
XTO32K	32 kHz Crystal oscillator

GENERAL DESCRIPTION

The ADF7242 is a fully integrated low-cost, short-range, low-power transceiver for operation in the global 2.4 GHz ISM-band. The ADF7242 has been designed with emphasis on flexibility, ease of use and low current consumption. The receive path is based on a zero-IF architecture enabling high blocking and selectivity performance. The transmit path is based on a direct closed loop VCO modulation scheme. The ADF7242 features an excellent performance versus power consumption metric making it especially suitable for battery powered systems.

The ADF7242 complies with the IEEE 802.15.4 –2006 2.4 GHz PHY requirements with a fixed net datarate of 250 kbps and DSSS-OQPSK modulation. With GFSK/FSK modulation the ADF7242 also supports a wide range of datarates, and is hence equally suitable for proprietary applications in the areas of industrial control, home and building automation as well as consumer electronics. The agile frequency synthesizer of the ADF7242 together with short turnaround times facilitates the implementation of FHSS transmission systems.

The ADF7242 features a flexible dual port RF-interface with support for switched antenna diversity. Also an integrated biasing circuit is provided to significantly simplify the interface to external PAs.

In order to optimise the system power consumption, the IC features an integrated low power RC-wake-up oscillator, which is calibrated off the high frequency crystal oscillator while the transceiver is active. Alternatively an integrated 32 kHz crystal oscillator may be used as a wake-up timer for applications requiring a highly accurate time base.

The ADF7242 is equipped with a SPI interface. The interface allows burst-mode data transfer for high throughput efficiency. A total of 256 bytes of TX_BUFFER and RX_BUFFER are provided to decouple the over-the-air data rate from the MCU processing speed. Support for automatic packet handling is integrated on-chip.

Alternatively for GFSK/FSK a synchronous bi-directional serial port (SPORT) provides bit-level data output, and has been designed to directly interface to wide range DSPs, such as ADSP-21xx, SHARC, TigerSHARC, and Blackfin. The SPORT interface may optionally be used for IEEE 802.15.4 data transfer also.

The IC is designed to achieve compliance with the following standards with a minimum number of external components: FCC CFR47 part 15, ETSI EN 300 440 (equipment class 2 – medium reliability), ETSI EN 300 328 (FHSS, DR > 250 kb/s) and ARIB STD T-66.

PACKET HANDLING SUPPORT

The ADF7242 provides hardware support for IEEE 802.15.4 packet oriented radio protocols. In transmit mode, the packet handler can be configured to process the payload data frame stored in the TX_BUFFER:

- Addition of preamble
- Addition of SFD
- Addition of FCS

In receive mode, the packet handling support helps to reconstruct the data frame:

- Detection of SFD
- Automatic FCS check

SPECIFICATIONS

V_{DDBAT} = 1.8 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.
Typical specifications are at V_{DDBAT} = 3 V, T_A = 25°C, f_{RF} = 2450 MHz.
All measurements are performed using the ADF7242 reference design, port 2, unless otherwise noted.

Table 1

Parameter	Min	Typ	Max	Unit	Test Conditions
GENERAL PARAMETERS					
Voltage Supply Range					
V_{DDBAT} Input	1.8		3.6	V	
Frequency Range	2400		2483.5	MHz	
Operating Temperature Range	–40		+85	°C	
Data rate	62.5		2000	kbps	GFSK/FSK mode
Data rate		250		kbps	IEEE 802.15.4 mode
Channel centre frequency control resolution			10	kHz	
TRANSMIT PATH					
Transmit Power	–20		+5	dBm	f_{RF} = 2450 MHz, V_{DDBAT}=3.0 V, T_A = 25°C;
Transmit Power Variation					
Condition 1		2		dB	f_{RF} = 2400 MHz to 2483.5 MHz, T_A = -40°C to +85°C, V_{DDBAT}=2.0 V to 3.6V
Condition 2		4		dB	f_{RF} = 2400 MHz to 2483.5 MHz, T_A = -40°C to +85°C, V_{DDBAT}=1.8V to 3.6V
Transmit Power Control Resolution		2		dB	
Harmonics and Spurious Emissions					
Compliant with ETSI EN 300 440					
25 MHz to 30 MHz			-36	dBm	Unmodulated carrier, 10 kHz RBW
30 MHz to 1 GHz			-36	dBm	unmodulated carrier, 100 kHz RBW
47 – 74, 87..5 – 118, 174 – 230, 470 – 862 MHz			-54	dBm	unmodulated carrier, 100 kHz RBW
Otherwise above 1 GHz			-30	dBm	unmodulated carrier, 1 MHz RBW
Compliant with ETSI EN 300 328					
1800 – 1900 MHz, 5150 – 5300 MHz			-47 -97	dBm dBm/Hz	unmodulated carrier
Compliant with FCC CFR47-15					
4.5 GHz – 5.15 GHz			-41	dBm	1 MHz RBW
7.25 GHz – 7.75 GHz			-41	dBm	1 MHz RBW
Optimum RFIO 2 Matching Impedance		tbd		Ω	Presented by matching network to RFIO2 differentially
TRANSMIT PATH IEEE 802.15.4 mode					
Transmit EVM		8		%	
Transmit PSD mask		-53		dBm	RBW=100 kHz; $\|f-f_{RF}\|$ > 3.5 MHz
TRANSMIT PATH GFSK/FSK mode					
Transmit MER		tbd		dB	GFSK 125 kbps, f_{dev}=60 kHz
Adjacent Channel Power N+/-1		tbd		dBc	GFSK 125 kbps, f_{dev}=60 kHz, meas BW = 250 kHz, 300 kHz channel spacing
Alternate Channel Power N+/-2		tbd		dBc	GFSK 125 kbps, f_{dev}=60 kHz, meas BW = 250 kHz, 300 kHz channel spacing
Occupied Power Bandwidth		tbd		kHz	GFSK 125 kbps, f_{dev}=60kHz, 99% power bandwidth

Parameter	Min	Typ	Max	Unit	Test Conditions
RECEIVE PATH IEEE 802.15.4 mode					
Sensitivity ($P_{in,min}$),		-97		dBm	1% PER PSDU length 20 bytes
Phase noise, >±50 MHz offset		-145		dBc/Hz	
Inband phase jitter			tbd	°	integrated from 10 kHz to 1.2 MHz
IIP3, LNA+MIX, max. gain		-18		dBm	f_{RF1} offset = 5 MHz; f_{RF2} offset = 10 MHz
Rx LO level at LNA/PA port		-100		dBm	measured at antenna port into 50 Ω
Rx Spurious Emissions					
Compliant with EN 300 440					
30 MHz – 1000 MHz			-57	dBm	at antenna i/p; narrowband
1 GHz – 12.75 GHz			-47	dBm	at antenna i/p; narrowband
RSSI, Dynamic range		85		dB	
Accuracy		±3		dB	
Averaging time		128		µs	
Minimum sensitivity		-95		dBm	
Frequency error tolerance	-80		80	ppm	$P_{in}=P_{in,\ min}+3$ dB
Optimum LNA Impedance		tbd		Ω	Presented by matching network to RFIO1 differentially
Channel 3 dB bandwidth		2600		kHz	analog and digital filter cascaded
Co-channel Rejection		-6		dB	$P_{in}=P_{in,\ min}+10$ dB
Adjacent channel Rejection					$P_{in}=P_{in,\ min}+3$ dB
N±1		46		dB	
N±2		54			
RX spurious reception		tbd		dB	Ratio of interferer to wanted signal for PER < 1%; wanted signal 10dB above sensitivity; CW interferer swept from 2400 MHz to 2483.5 MHz excluding +/-5 MHz region centered around wanted signal.
Blocking Resilience					
±5 MHz		-40		dBm	$P_{in}=P_{in,min}+3$ dB; CW blocker
±10 MHz		-35		dBm	$P_{in}=P_{in,min}+3$ dB; CW blocker
±20 MHz		-27		dBm	$P_{in}=P_{in,min}+3$ dB; CW blocker
±50 MHz		-27		dBm	$P_{in}=P_{in,min}+3$ dB; CW blocker
RECEIVE PATH GFSK mode					
Sensitivity (Pin,min), 0.1 % BER					
2 Mbps, GFSK		-84		dBm	f_{dev} = ±500 kHz
1 Mbps, GFSK		-87		dBm	f_{dev} = ±250 kHz
500 kbps, GFSK		-90		dBm	f_{dev} = ±130 kHz
250 kbps, GFSK		-93		dBm	f_{dev} = ±130 kHz
125 kbps, GFSK		tbd		dBm	f_{dev} = ±60 kHz
Saturation level		-15		dBm	0.1 % BER (all modulation schemes)
Channel 3 dB bandwidth	500		2600	kHz	analog and digital filter cascaded
Co-channel Rejection		-11		dB	DR=250 kbps (GFSK); $P_{in}=P_{in,min}+10$ dB
Adjacent Channel Rejection					$P_{in}=P_{in,min}+10$ dB; 500 kHz channel spacing; 250 kbps GFSK, fdev=130 kHz
N±1		15		dB	
N±2		20		dB	
Blocking Resilience					
±5 MHz		-40		dBm	$P_{in}=P_{in,min}+3$ dB; CW blocker

Parameter	Min	Typ	Max	Unit	Test Conditions
±10 MHz		-35		dBm	$P_{in}=P_{in,min}$+3 dB; CW blocker
±20 MHz		-27		dBm	$P_{in}=P_{in,min}$+3 dB; CW blocker
±50 MHz		-27		dBm	$P_{in}=P_{in,min}$+3 dB; CW blocker
RX and TX TIMING PARAMETERS IEEE 802.15.4 mode					
IDLE to PHY_RDY state		142	150	µs	
PHY_RDY or TX to RX (different channel)	181	192		µs	VCO calibration performed
PHY_RDY or RX to TX (different channel): t_{18}	160	192		µs	VCO calibration performed
PHY_RDY or TX to RX (same channel)	129			µs	VCO calibration skipped
RX or PHY_RDY to TX (same channel)	108			µs	VCO calibration skipped
RX channel change	181	192		µs	full RX path calibration
TX channel change	160	192		µs	full Tx path calibration
RX and TX TIMING PARAMETERS GFSK/FSK mode					
IDLE to PHY_RDY state		142	150	µs	
PHY_RDY or TX to RX (different channel)	320			µs	VCO calibration performed
PHY_RDY or RX to TX (different channel)	166			µs	VCO calibration performed
PHY_RDY or TX to RX (same channel)	268			µs	VCO calibration skipped
RX or PHY_RDY to TX (same channel)	114			µs	VCO calibration skipped
RX channel change	320			µs	full RX path calibration
TX channel change	166			µs	full Tx path calibration
CRYSTAL OSCILLATOR					
Crystal frequency		26		MHz	parallel mode
Crystal ESR			1800	Ω	
SLEEP to IDLE wake-up time		300		µs	Load capacitance
RC OSCILLATOR					
Frequency		32.768		kHz	after calibration
Frequency accuracy		tbd		ppm	after calibration
Frequency drift					
Temperature coefficient		tbd		% / °C	
Voltage coefficient		tbd		% / V	
Calibration time			1	ms	
Wakeup period	61e-6		131e3	s	programmable
32kHz XTAL OSCILLATOR					
Frequency		32.768		kHz	
Frequency accuracy		tbd		ppm	
ESR			tbd		
Start-up time			2000	ms	
WAKE-UP TIMER					
Prescaler Tick Period	0.0305		20000	ms	
Wake-up period	61e-6		1.31e5	s	
TEMPERATURE SENSOR					
Range	-40		+85	°C	
Resolution				°C	
Accuracy (Uncalibrated)		tbd		°C	At 25°C

Parameter	Min	Typ	Max	Unit	Test Conditions
BATTERY MONITOR					
Relative accuracy	-8		+8	%	
Toggle voltage range	1.7		3.6	V	
Toggle voltage step size		62		mV	
Startup time			5	µs	
EXTERNAL PA INTERFACE					
Ron, PA_VSUP to VDDBAT		5		Ω	extpa_bias_mode= 0, 1, 2, 8, 9 , 10
Roff, PA_VSUP, to GND		10		MΩ	extpa_bias_mode= 3, 4, 11, 12, power dn
Roff, PA_BIASOP to GND		10		MΩ	extpa_bias_mode=0, power down
PA_BIASOP source current, max		80		µA	expta_bias_mode = 1, 3
PA_BIASOP sink current, min		-80		µA	extpa_bias_mode = 2, 4
PA_BIASOP current control resolution		6		bits	extpa_bias_mode = 1, 2, 3, 4, 5
PA_BIASOP compliance voltage	tbd			V	extpa_bias_mode = 2, 4
PA_BIASOP, compliance voltage			tbd	V	extpa_bias_mode = 3, 4
Servo loop bias current	0		23.6	mA	extpa_bias_mode = 5, 6
Servo loop bias current control step		0.369		mA	extpa_bias_mode = 5, 6
Servo loop bias absolute accuracy	tbd		tbd	%	extpa_bias_mode = 5, 6
CURRENT CONSUMPTION					
TX mode current consumption					
−20 dBm		tbd		mA	
−10 dBm		tbd		mA	
0 dBm		tbd		mA	
3 dBm		22		mA	
5dBm		tbd		mA	
PHY_RDY mode		10.7		mA	
RX mode current consumption		18		mA	IEEE 802.15.4 Mode
SLEEP		0.15		µA	deep sleep mode
SLEEP_BBRAM		0.25		µA	BBRAM contents retained
SLEEP_BBRAM_RCO		0.6		µA	RCO32K running; BBRAM contents retained
SLEEP_BBRAM_XTO		1.25		µA	XTO32K running; BBRAM contents retained
IDLE mode		2.4		mA	XTO26M + digital active
BATTMON		30		µA	when enabled

Digital Logic and TIMING CHARACTERISTICS

Table 2: Logic Levels

Parameter	Min	Typ	Max	Unit	Test Conditions
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DDBAT}			V	
Input Low Voltage, V_{INL}			0.2 × V_{DD}	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DDBAT} − 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
Output Rise/Fall			5	ns	
Output Load			7	pF	

Table 3: SPI Interface timing

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$t_{1active}$			15	ns	CSN falling edge to SO setup time (TRX active)
t_{1Wake_up}		300	400	µs	SLEEP to IDLE state (CSN low to SO high)
t_2	40			ns	CSN to SCLK setup time
t_3	40			ns	SCLK high time
t_4	40			ns	SCLK low time
t_5	80			ns	SCLK period
t_6			10	ns	SCLK falling edge to SO delay
t_7	5			ns	SI to SCLK rising edge setup time
t_8	5			ns	SI to SCLK rising edge hold time
t_9	40			ns	SCLK to CSN hold time
t_{10}	10			ns	CSN high to SCLK wait time
t_{11}	270			ns	CSN high time

Table 4: MAC Timing Delay

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
T_{27}			150	µs	Time allowed, from issuing a RC_TX command, to update delay_cfg2.mac_delay_ext Register
T_{28}			150	µs	Time allowed, from issuing a RC_TX command, to cancel the RC_TX command

Table 5: Timing IEEE 802.15.4 SPORT mode

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_{21}	18			µs	SFD detect to (TRCLK_CLKO_GP3) active delay
t_{22}		2		µs	TRCLK_CKO_GP3 period
t_{23}	510			ns	DR_GP0 to TRCLK_CKO_GP3 falling edge setup time
t_{24}		16		µs	TRCLK_CKO_GP3 symbol burst period
t_{25}		6		µs	TRCLK_CKO_GP3(data bit clock) to IRQ2_TRFS_GP2 (symbol clock)
t_{26}		0.5		µs	IRQ2_TRFS_GP2 high time

Table 6: Timing GFSK SPORT mode

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_{29}			12	µs	RC_PHY_RDY to TRCLK_CKO_GP3 (data clock) off
t_{30}	Tsym/2 - 30ns				DR_GP0 to TRCLK_CKO_GP3 active edge hold time
t_{31}	Tsym/2 - 30ns				DR_GP0 to TRCLK_CKO_GP3 active edge setup time
t_{32}		Tsym			TRCLK_CLKO_GP3 clock period
t_{33}	20			ns	DT_GP1 to TRCLK_CKO_GP3 sampling edge setup time
t_{34}	20			ns	DT_GP1 to TRCLK_CKO_GP3 sampling edge hold time
t_{35}	1.3		6.2	µs	PA nominal power to TRCLK_CKO_GP3 activity / entry into TX state
t_{36}			7.5	µs	RC_PHY_RDY to TRCLK_CLKO_GP3 off
t_{37}			12	µs	TRCLK_CKO_GP3 clock off to PA power shutdown
t_{38}	Tsym/2 – 60ns		Tsym/2		IRQ2_TRFS_GP3 rising edge to TRCLK_CKO_GP3 active edge delay
t_{39}	0			µs	DR_GP0 activity to end of sync word delay
t_{40}		5 * Tsym			
t_{41}		24 * Tsym + 25us			Start of preamble to TRCLK_CKO_GP3 activity delay
t_{42}		153		µs	RC_RX command to TRCLK_CKO_GP3 activity delay (calibrations performed)

Timing Diagrams

SPI Interface Timing diagrams

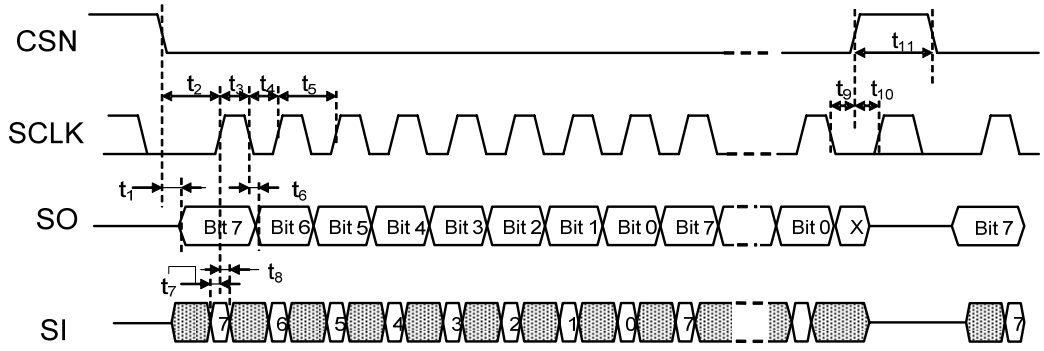


Figure 2: SPI Interface timing

Note further timing diagrams available under the Serial Control interfacesection

State transition timing

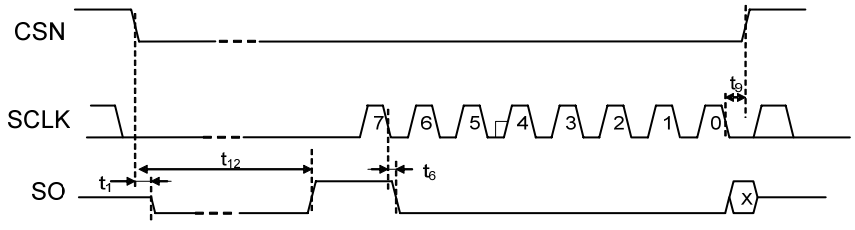


Figure 3: SLEEP to IDLE state timing

SPORT Interface Timing diagrams

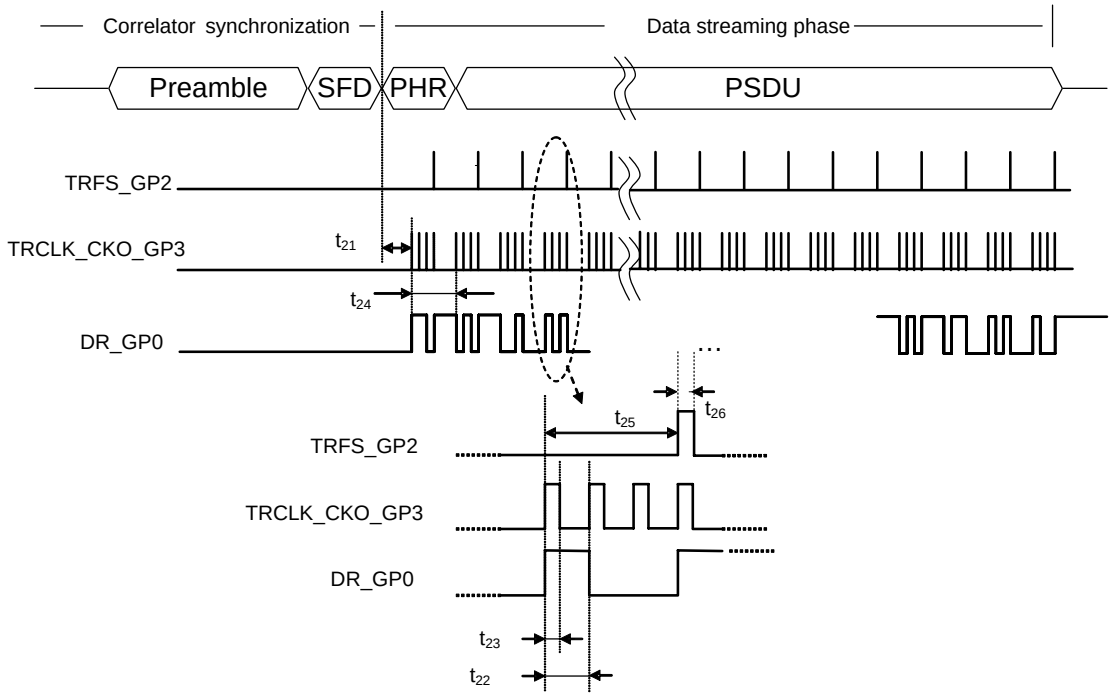


Figure 4: RX-mode IEEE 802.15.4 SPORT mode with packet handler enabled (rc_cfg.rc_mode=0, , gp_cfg.gpio_cfg=1)

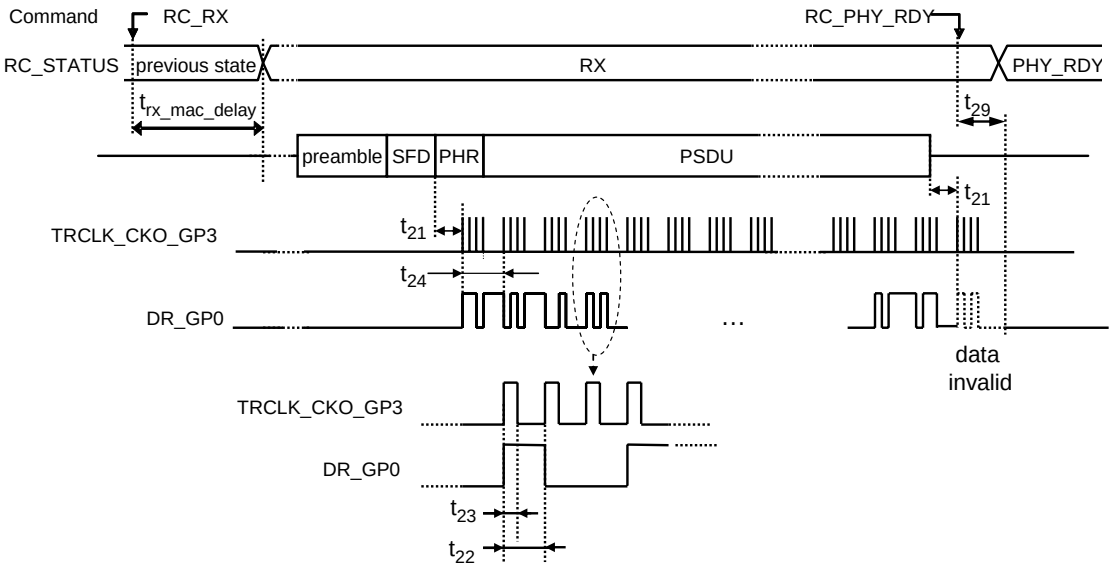


Figure 5: IEEE802.15.4 Rx SPORT mode rc_cfg.rc_mode=2, gp_cfg.gpio_cfg=3

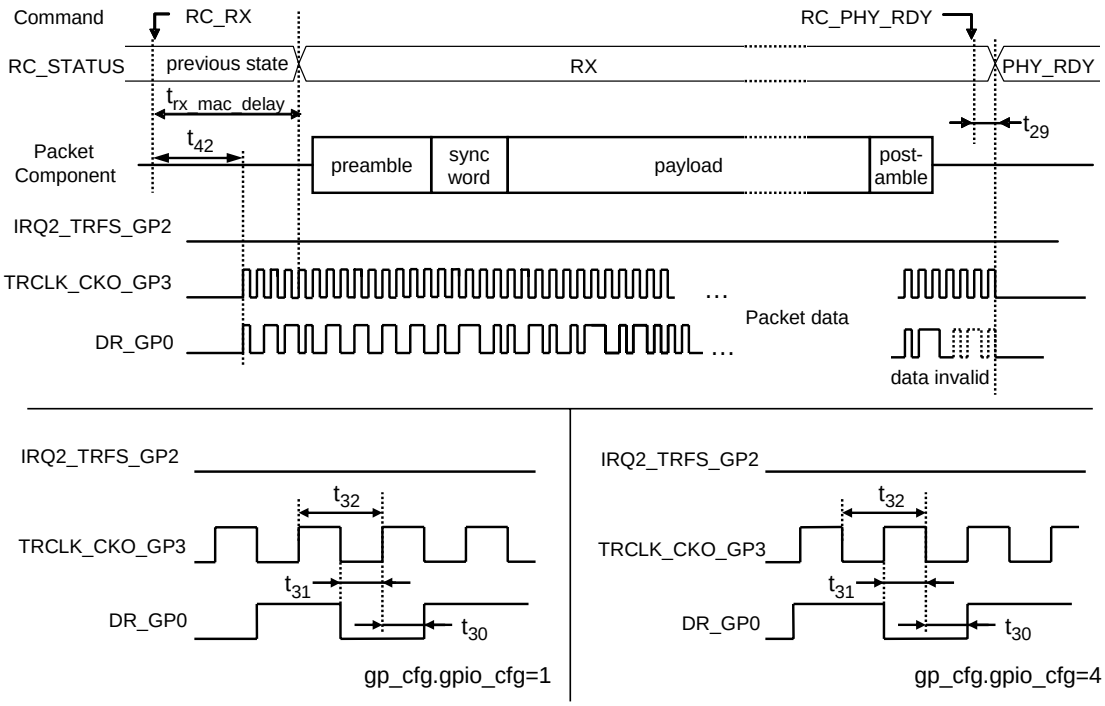


Figure 6: GFSK/FSK Rx SPORT mode gp_cfg.gpio_cfg=1 and gp_cfg.gpio_cfg=4

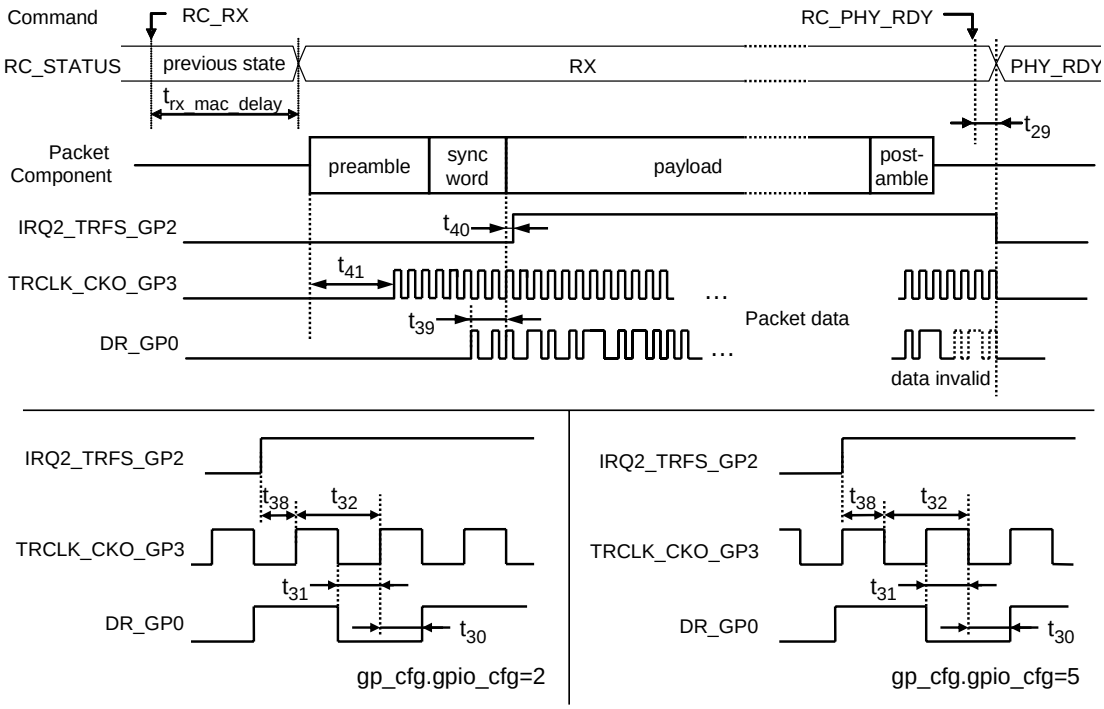


Figure 7: GFSK/FSK Rx SPORT mode gp_cfg.gpio_cfg=2 and gp_cfg.gpio_cfg=5

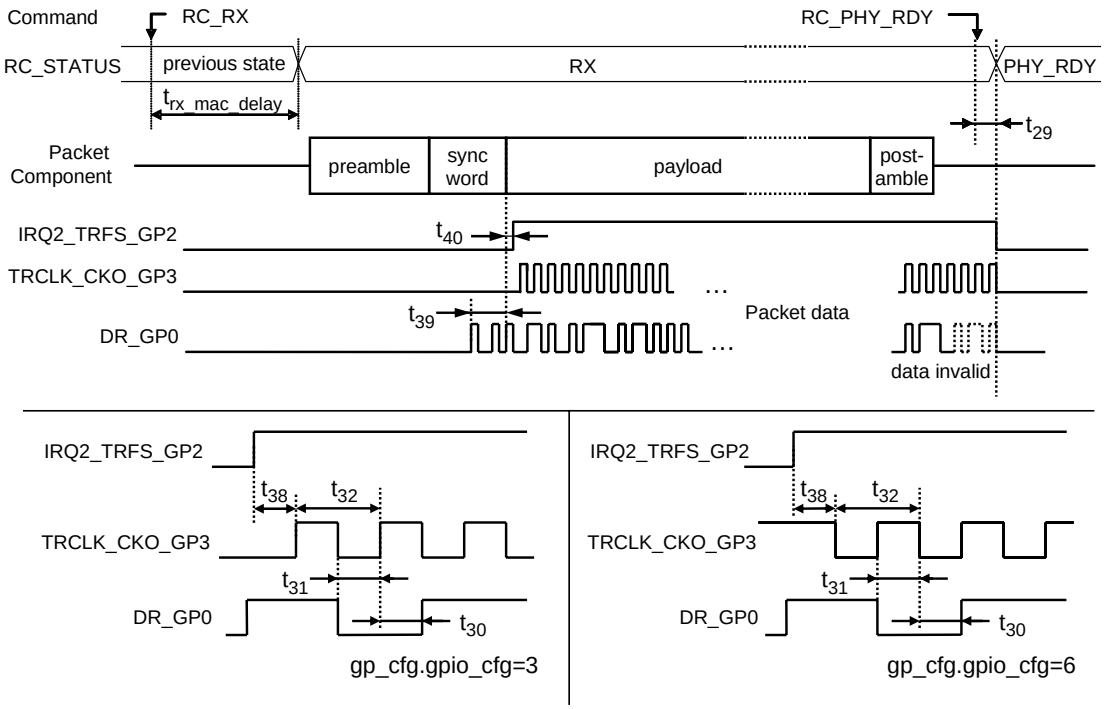


Figure 8: GFSK/FSK Rx SPORT mode gp_cfg.gpio_cfg=3 and gp_cfg.gpio_cfg=6

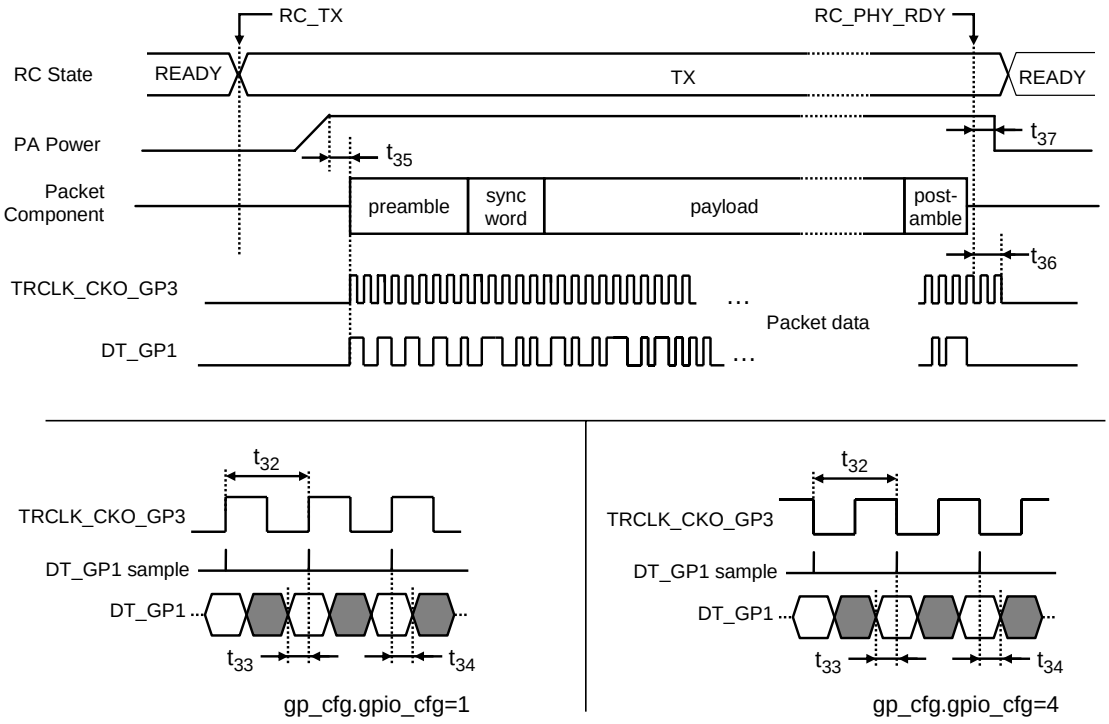


Figure 9: GFSK/FSK TX SPORT mode gp_cfg.gpio_cfg=1 and gp_cfg.gpio_cfg=4

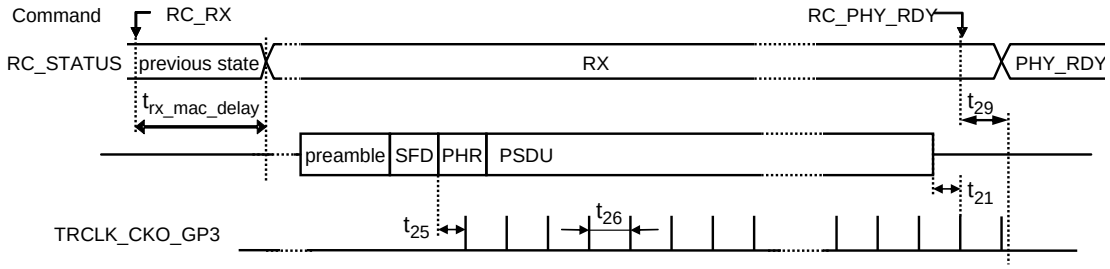


Figure 10: IEEE802.15.4 SPORT symbol clock output mode (rc_cfg.rc_mode=0, gp_cfg.gpio_cfg=7)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7

Parameter	Rating
V_{DD} to GND	−0.3 V to +3.6 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
MLF θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40sec

The exposed paddle of the LFCSP package should be connected to ground.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

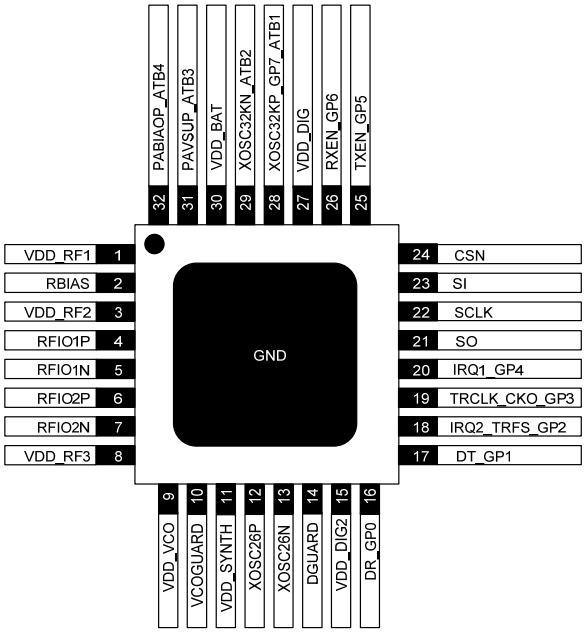


Figure 11. Pin configuration ADF7242 (LFCSP-32)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VDD_RF1	Regulated supply terminal for RF section. Blocking capacitor 220 nF to GND
2	RBIAS	Bias resistor 27 kΩ to GND
3	VDD_RF2	Regulated supply for RF section. Blocking capacitor 100 pF to GND
4	RFIO1P	Differential RF input port 1 (positive terminal).
5	RFIO1N	Differential RF input port 1 (negative terminal).
6	RFIO2P	Differential RF input/output port 2 (positive terminal)
7	RFIO2N	Differential RF input/output port 2 (negative terminal)
8	VDD_RF3	Regulated supply for RF section. Blocking capacitor 100 pF to GND
9	VDD_VCO	Regulated supply for VCO section. Blocking capacitor 220 nF to GND
10	VCOGUARD	Guard trench for VCO section. Connect to pin 9 (VDD_VCO)
11	VDD_SYNTH	Regulated supply for PLL section. Blocking capacitor 220 nF to GND
12	XOSC26P	Terminal 1 of external crystal and loading capacitor. NC when an external oscillator is used.
13	XOSC26N	Terminal 2 of external crystal and loading capacitor. Input for external oscillator.
14	DGUARD	Guard trench for digital section. Connect to pin 15 (VDD_DIG2)
15	VDD_DIG2	Regulated supply for digital section. Blocking capacitor 220 nF to GND
16	DR_GP0	SPORT receive data output /general purpose IO port
17	DT_GP1	SPORT Transmit data input /general purpose IO pin
18	IRQ2_TRFS_GP2	Interrupt request output 2/symbol clock IEEE 802.15.4 mode/general purpose IO port
19	TRCLK_CKO_GP3	SPORT clock output /general purpose IO port.
20	IRQ1_GP4	Interrupt request output1 / general purpose IO port.
21	SO	SPI interface serial data output
22	SCLK	SPI interface data clock input
23	SI	SPI interface serial data input
24	CSN	SPI interface chip select input (and wake-up signal)
25	TXEN_GP5	External PA enable signal / general purpose IO port
26	RXEN_GP6	External LNA enable signal / general purpose IO port

Pin No.	Mnemonic	Function
27	VDD_DIG	Regulated supply for digital section. Blocking capacitor 1 nF to GND
28	XOSC32KP_GP7_ATB1	Terminal 1 of 32 kHz crystal oscillator / general purpose IO port / analog test bus 1
29	XOSC32KN_ATB2	Terminal 2 of 32 kHz crystal oscillator / analog test bus 2
30	VDD_BAT	Unregulated supply input from battery.
31	PAVSUP_ATB3	External PA supply terminal / analog test bus 3
32	PABIAOP_ATB4	External PA bias voltage output / analog test bus 4
paddle	GND	Common ground terminal.

RADIO CONTROL STATES

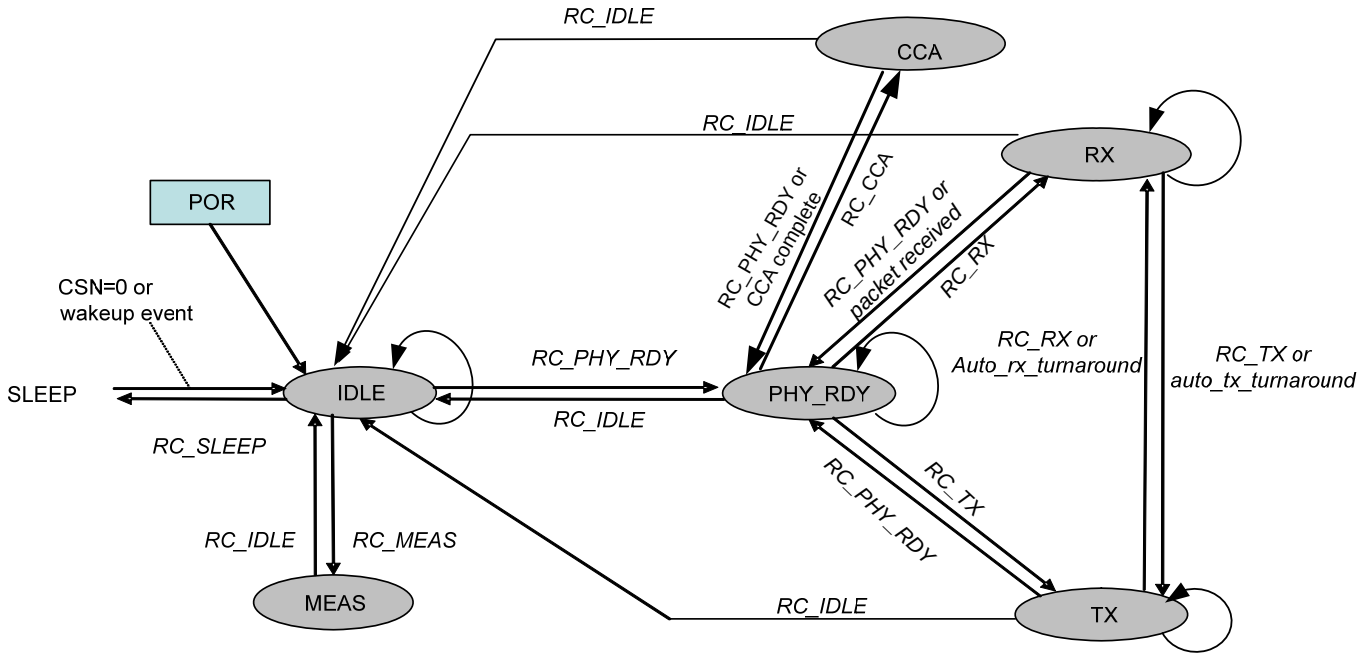


Figure 12: ADF7242 state diagram

OPERATIONAL STATES

A power on reset (POR) occurs when the battery voltage is first applied to the ADF7242. All LDOs are enabled together with the 26 MHz crystal oscillator and the digital core. After initializing configuration registers to their default values, the ADF7242 enters IDLE state.

IDLE state - All analog blocks required for radio operation are powered down. The digital section is enabled and all configuration registers as well as the RX_BUFFER and TX_BUFFER are fully accessible. It is appropriate for the MCU to set any configuration parameter, such as modulation scheme, channel frequency, and WUC configuration in this state. IDLE state may also be entered by issuing an RC_IDLE command in any state other than SLEEP. Bringing the CSN input low in SLEEP state causes a transition into IDLE state.

PHY_RDY state – Upon entering PHY_RDY state from IDLE state the synthesizer is enabled and required system calibration procedures are carried out. The calibration is omitted when the PHY_RDY state is entered from RX, TX or CCA. PHY_RDY state may be entered from states IDLE, RX, TX or CCA by issuing an RC_PHY_RDY command.

RX state – The synthesizer is automatically calibrated to the current frequency control word upon entering the RX state from states PHY_RDY or TX. The synthesizer calibration may be omitted for single channel communication systems if short turnaround times are required. Following a programmable rx_mac_delay period, the ADF7242 starts searching for an SFD/sync word. RX state can be entered from states PHY_RDY and TX by issuing an RC_RX command. If buffercfg.rx_buffer_mode=0 then the part reverts automatically to PHY_RDY once an rx_pkt_rcvd interrupt condition occurs. If buffercfg.rx_buffer_mode=1 the part remains in RX state until a command to enter a different state is issued.

CCA state- Upon entering the CCA state a clear channel assessment is executed. Per default on completion the ADF7242 reverts to PHY_RDY state.

TX state– Upon entering the TX state the synthesizer is automatically calibrated to the current frequency control word. The synthesizer calibration may be omitted for communication systems operating on a single channel if short turnaround times are required. Following a programmable delay period, the PA is enabled, and transmission is initiated. TX state can be entered from states PHY_RDY or RX by issuing a RC_TX command.

MEAS state – This state is enabled by issuing a RC_MEAS command. The Tx/Rx functionality is disabled and the ADC is used to measure the chip temperature. The result may be read from register adc_rbk.adc_out which is continuously updated.

SLEEP state – The SLEEP state is invoked with the RC_SLEEP command. The SLEEP state can be configured to operate in five different modes, which are listed in Table9.

Table 9: ADF7242 SLEEP modes

SLEEP mode	Circuits active	Functionality
SLEEP_DEEP	None	None – Packet RAM content and MCR settings, with the exception of the wake up configuration shadow register, are not maintained
SLEEP_BBRAM	BBRAM[1]	Wake up configuration shadow register and BBRAM configuration settings maintained. Packet RAM and MCRs contents not maintained.
SLEEP_XTO	XTO	As for mode SLEEP but XTO32K is enabled
SLEEP_BBRAM_XTO	BBRAM[1] XTO32K	As for mode SLEEP_XTO with data retention in BBRAM
SLEEP_BBRAM_RCO	BBRAM RCO32K	As for mode SLEEP_BBRAM_XTO but using RCO32K instead.

The CSN input must be kept high while the ADF7242 is in SLEEP state. SLEEP state may be exited either by bringing the CSN input low or by a time-out event with the WUC configured.

SLEEP MODES

The SLEEP modes are configurable with the wake up configuration registers, tmr_cfg0 and tmr_cfg1. The wake up configuration registers have shadow registers with battery backup, which are only updated after register tmr_cfg1 has been written to. The contents of register tmr_cfg0 and tmr_cfg1 are reset in SLEEP state while the previously programmed values are still maintained in the shadow registers and continue to prevail.

SLEEP_DEEP is the mode with the lowest power consumption. It is suitable for use in applications where a wake-up timer and non-volatile memory is available in the MCU. SLEEP_DEEP is the default sleep mode selected after a POR.

SLEEP_BBRAM mode is suitable for applications where the MCU is equipped with its own wake-up timer, but has no non-volatile memory. SLEEP_BBRAM mode is enabled through setting tmr_cfg1.sleep_config=1.

SLEEP_XTO mode enables the XTO32K and the WUC. It is enabled through setting tmr_cfg1.sleep_config=4. SLEEP_XTO mode allows the generation of a wakeup interrupt for the MCU when a programmed timeout period has elapsed.

SLEEP_BBRAM_XTO mode has the functionality of mode SLEEP_XTO and also retains data in the BBRAM during SLEEP state. In order to enable SLEEP_BBRAM_XTO mode, set tmr_cfg1.sleep_config= 5 and enable RTC interrupt by setting irqx_en0.wakeup=1. Please refer to section Wake up timer for details on how to configure the ADF7242 WUC.

SLEEP_BBRAM_RCO mode is as per SLEEP_BBRAM_XTO except the timer unit is clocked by RCO32K rather than XTO32K. This may be used when lower timer accuracy is acceptable. It is enabled through setting tmr_cfg1.sleep_config=11.

Note:

[1] BBRAM: The BBRAM includes configuration settings such as the interrupt configuration which will be maintained in SLEEP_BBRAM mode.

SYNTHESIZER

FREQUENCY PROGRAMMING

The frequency of the synthesizer is programmed with the frequency control word ch_freq[23:0], which extends over registers ch_freq0, ch_freq1, and ch_freq2. The frequency control word ch_freq[23:0] contains a binary representation of the absolute frequency of the desired channel divided by 10 kHz. There is no difference between the setting required for Rx and Tx operation.

Writing a new frequency value to the frequency control word ch_freq[23:0] takes effect after the next synthesizer calibration. The synthesizer is calibrated by default during the transition into PHY_RDY, TX and RX state. Please refer to sections

Tx Path and Synthesizer Calibration and Rx Path Calibration for details. In order to facilitate fast channel changes, a new frequency control word may be written in RX state before a packet has been received. The next RC_RX or RC_TX command will then initiate the required synthesizer calibration. Similarly a new frequency control word may be written after a packet has been transmitted while in TX state. The next RC_RX or RC_TX command initiates the synthesizer calibration cycle required to re-lock the synthesizer.

CRYSTAL OSCILLATOR

The on-chip crystal oscillator generates the reference frequency for the synthesizer and system timing. The oscillator operates at a frequency of 26 MHz. The crystal oscillator is amplitude controlled in order to ensure a fast start-up time and stable operation under different operating conditions. The crystal and associated external components should be chosen with care since the accuracy of the crystal oscillator can have a significant impact on the performance of the communication system. Apart from the accuracy and drift specification, it is important to consider the nominal loading capacitance. Crystals with a high loading capacitance are less sensitive to frequency pulling due to tolerances of external components and parasitics. On the other hand, a larger loading capacitance results in a higher current consumption, longer start-up time and lower trimming range.

The total loading capacitance must be equal to the specified load capacitance of the crystal, and is comprised of the external parallel loading capacitors, the parasitic capacitances of pins XOSC26P and XOSC26N, as well as the parasitic capacitance of tracks on the printed-circuit board.

The ADF7242 has an integrated crystal oscillator tuning capacitor, which facilitates the compensation of systematic production tolerances, and temperature drift. The tuning capacitor is controlled with register synt_cal.xto26_trim. The tuning range provided by the tuning capacitor depends on the loading capacitance of a specific crystal, and is typically on the order of 25 ppm.

TRANSMITTER

MODULATION SCHEMES

The ADF7242 supports IEEE 802.15.4 compliant DSSS-OQPSK modulation with a bitrate of 250 kbps. The ADF7242 also supports FSK and GFSK modulation with bitrates from 62.5 kbps to 2 Mbps. Table 10 lists recommended modulation parameters. The setting of register rc_cfg.rc_mode controls whether the ADF7242 operates in one of the IEEE802.15.4 modes or GFSK/FSK mode. The data rate DR is set with registers dr0.data_rate_high and dr1.data_rate_low according to the following equation:

DR= (dr0.data_rate_high * 256 + dr1.data_rate_low) * 100b/s

The default values of registers dr0 and dr1 configures the correct setting for IEEE 802.15.4 mode. Please note the ADF7242 fully supports arbitrary data rates only for FSK mode of operation. For GFSK mode of operation only the data rates listed in Table 10 are supported.

For data rates greater than 250 kbps, and IEEE 802.15.4 mode, the modulator preemphasis filter must be enabled with tx_m.preemp_filt=1. Spectral efficiency is often desirable for narrowband communication systems using FHSS. The modulator of the ADF7242 has an optional Gaussian symbol filter, which can be enabled with configuration bit tx_m.gauss_filt=1. The BT product of the Gaussian symbol filter is 0.5 and cannot be changed. Gaussian filtering must be disabled for IEEE 802.15.4 mode.

The deviation frequency (Fdev) of the modulator is programmable with register tx_fd.tx_freq_dev in steps of 10 kHz. The register map shows recommended settings for register tx_fd.tx_freq_dev corresponding with the recommended modulation parameters listed in Table 10. The default value of register tx_fd.tx_freq_dev configures the correct setting for IEEE 802.15.4 mode.

Table 10: ADF7242 recommended modulation schemes

Bitrate [kbps]	Modulation Type	Comment
250	DSSS-OQPSK	IEEE 802.15.4 compliant
62.5	GFSK / FSK	Fdev = ±60 kHz
125	GFSK / FSK	Fdev = ±60 kHz
250	GFSK / FSK	Fdev = ±130 kHz
500	GFSK / FSK	Fdev = ±250 kHz
1000	GFSK / FSK	Fdev = ±250 kHz
2000	GFSK / FSK	Fdev = ±500 kHz

TX PATH AND SYNTHESIZER CALIBRATION

The radio section of the ADF7242 requires a system calibration prior to being useable for receive or transmit operation. Since the calibration information is lost when the ADF7242 enters IDLE state, a full system calibration is automatically performed on the transition between IDLE and PHY_RDY state. The system calibration is omitted when PHY_RDY state is entered from eitherTX, RX or CCA state.

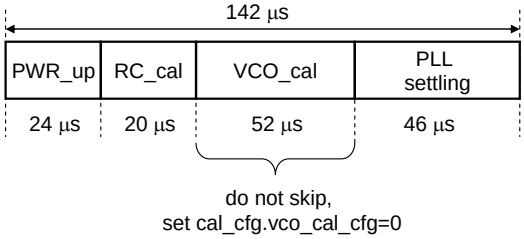


Figure 13: System calibration following RC_PHY_RDY

Figure 13 illustrates the components of the system calibration cycle. It comprises a calibration of the RX baseband filter (RC_cal) and the VCO band (VCO_cal) followed by a PLL settling phase. The calibration step VCO_cal must not be skipped during the system calibration. Hence it is important to ensure that cal_cfg.vco_cal_cfg = 0 prior to entering PHY_RDY state from IDLE. This is the default state and therefore only requires programming if skipping of the VCO_cal was previously selected.

IEEE802.15.4 TX TIMING AND CONTROL

This section applies when IEEE 802.15.4 frame mode has been enabled (rc_cfg.rc_mode=0). Accurate control over the transmission slot timing is maintained by two delay timers (delay_cfg1 .tx_mac_delay and delay_cfg2 .mac_delay_ext), which introduces a controlled delay between the rising edge of the CSN signal following the RC_TX command and the start of the transmit operation. Figure 14 illustrates the timing of the TX operation assuming that the ADF7242 was operating in PHY_RDY, RX or TX state prior to the execution of an RC_TX command.

If enabled the external PA interface is powered up prior to the synthesizer calibration in order to allow sufficient time for the bias servo to settle. Ramp-up of the PA is completed shortly before the overall MAC delay has elapsed. Following the completion of the PA ramp-up phase the transceiver enters TX state. The minimum and maximum time for the PA ramp-up to complete prior to the transceiver entering TX state given by parameter t35 in *Table 6* also applies to IEEE 802.15.4 TX mode. If enabled an rc_ready interrupt is generated at the transition point.

The radio controller first transmits the automatically generated preamble and SFD. If it has been enabled, an SFD interrupt is asserted at this point. The radio controller then reads the

TX_BUFFER starting with the PHR byte and transmits its contents. Following the transmission of the entire frame, the radio controller turns the PA off, and asserts a tx_pkt_sent interrupt. Unless automatic operating modes have been configured the ADF7242 then automatically returns to state PHY_RDY.

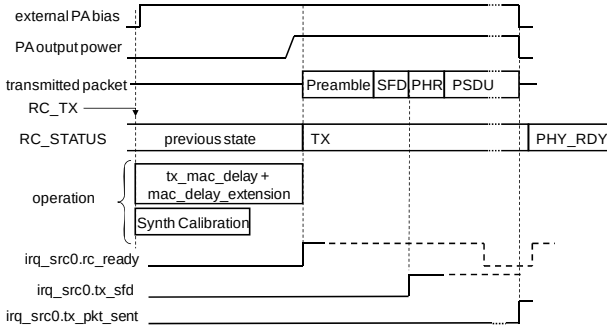


Figure 14: Tx Timing and Control (IEEE 802.15.4 mode)

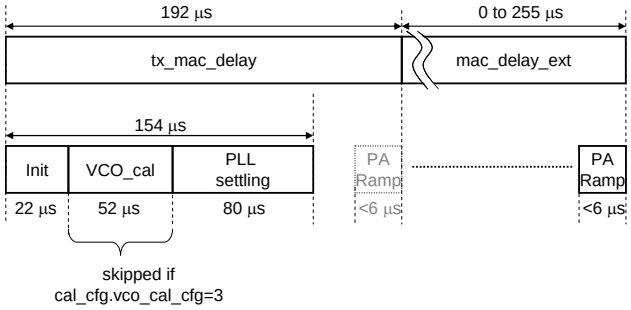


Figure 15: Synthesizer calibration following RC_TX

By default the synthesizer is re-calibrated each time an RC_TX command is issued. Figure 15 shows the synthesizer calibration sequence that is performed each time the transceiver enters TX state. The total Tx MAC delay is defined by the combined delay configured with registers delay_cfg1.tx_mac_delay and delay_cfg2.mac_delay_ext. Both delay registers are programmable in steps of 1 µs. The default value of register delay_cfg1.tx_mac_delay is the length of 12 IEEE 802.15.4-2.4GHz symbols or 192 µs. The default value of delay_cfg2.mac_delay_ext is 0 µs. Register delay_cfg2.mac_delay_ext may be updated up to the time specified by parameter t_{27} in Table *4* following the assertion of the RC_TX command while the delay defined by register delay_cfg1.tx_mac_delay is elapsing. This allows a dynamic adjustment of the transmission timing for ACK frames for networks using slotted CSMA/CA. In order to ensure correct settling of the synthesizer prior to PA ramp-up, the total Tx MAC delay should not be programmed to a value shorter than specified by the PHY_RDY or RX to TX timing specified in Table 1. The RC_TX command may be aborted up to the time specified by parameter t_{28} in Table *4* by means of issuing an RC_PHY_RDY, RC_RX or RC_IDLE command.

The VCO calibration (VCO_cal) may be skipped if shorter turn-around times are required. Skipping the VCO calibration is possible if the channel frequency control word ch_freq[23:0] has remained unchanged since the last RC_PHY_RDY, RC_RX, RC_CCA or RC_TX command has been issued with VCO_cal enabled. However, the initialization (Init), PLL settling and PA ramping phases are mandatory as the PLL bandwidth is changed between RX and TX operation. This is an option for single channel communication systems or the transmission of an ACK frame on the same channel. The VCO_cal is skipped if cal_cfg. vco_cal_cfg=3. In this case the tx_mac_delay may be reduced to 106 µs. The VCO calibration is executed if cal_cfg. vco_cal_cfg=0.

IEEE 802.15.4 TX PACKET MODE

IEEE 802.15.4 compatible mode with packet handler support is selected with rc_cfg.rc_mode=0. In this mode the ADF7242 radio controller automatically generates the IEEE 802.15.4 compatible preamble and SFD. The packet length (PHR) must be the first byte written to the TX_BUFFER. It is stored in location txpb.tx_packet_base. The format of the frame in the TX_BUFFER depends on whether the automatic FCS field generation has been disabled or not.

If the automatic FCS field generation has been disabled (pkt_cfg.auto_fcs_off=1), the full frame including FCS must be written to the TX_BUFFER. In this case, the number of bytes written to the TX_BUFFER must be equal to the length specified in the PHR field.

If the automatic FCS field generation has been enabled (pkt_cfg.auto_fcs_off=0), the FCS is automatically appended to the frame in the TX_BUFFER. In this case, the number of bytes written to the TX_BUFFER must be equal to the length specified in the PHR field minus two.

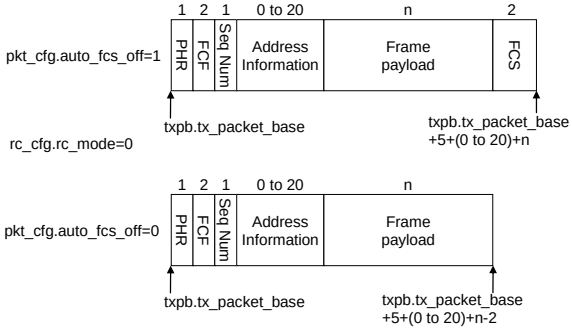


Figure 16: Frame format of TX_BUFFER

IEEE802.15.4 AUTO TX TURNAROUND MODE

The ADF7242 features an automatic Rx to Tx turnaround mode when it is operating in IEEE 802.15.4 packet mode (rc_cfg.rc_mode=0). The automatic Tx turnaround mode

facilitates the timely transmission of acknowledgement frames.

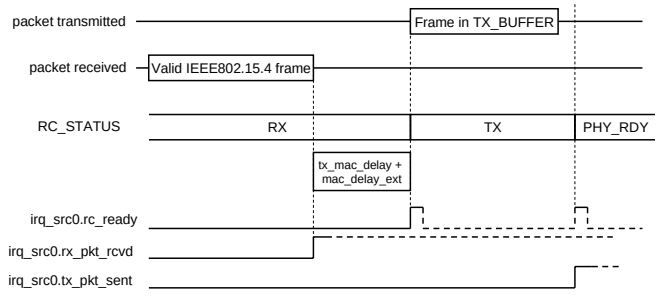


Figure 17: IEEE802.15.4 Auto Rx Turnaround Mode

Figure 17 illustrates the timing of the automatic Tx turnaround mode. When enabled by setting register bit buffer_cfg.auto_tx_turnaround the ADF7242 automatically enters TX state following the reception of a valid IEEE802.15.4 frame. After the combined Tx MAC delay (tx_mac_delay + mac_delay_ext) the ADF7242 is entering TX state and transmits the frame stored in the TX_BUFFER. After the transmission is complete, the ADF7242 enters PHY_RDY state. The user MCU has up to t_{28} after a frame has been received to cancel the TX operation by means of issuing an RC_IDLE, RC_PHY_RDY or RC_RX command.

GFSK/FSK TX TIMING AND CONTROL

For GFSK/FSK Tx operation (rc_cfg.rc_mode=3) the ADF7242 must be configured for SPORT operation. Please refer to section SPORT Interface for details.

Figure 18 illustrates the timing of the TX operation in GFSK/FSK Tx SPORT mode. Following the transition into TX state the radio controller starts to shift serial data from the SPORT interface into the modulator until the TX state is left with an appropriate command. Since the packet composition is entirely under user control, no tx_sfd and tx_pkt_sent interrupts are generated.

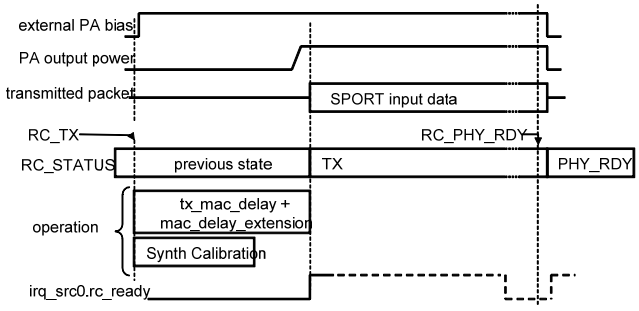


Figure 18: Tx Timing and Control (GFSK/FSK SPORT mode)

The calibration sequence shown in Figure 15 in section IEEE802.15.4 Tx Timing and Control is fully applicable for GFSK/FSK Tx SPORT mode.

POWER AMPLIFIER

The integrated power amplifier (PA) is connected to RF ports RFIO2P and RFIO2N. It is equipped with a built-in harmonic filter to simplify the design of the external harmonic filter. The output power of the PA is set with register extpa_msc.pa_pwr with a nominal step size of 2 dB. The step size increases at the lower end of the control range. The step size may decrease at the upper end of the control range due to compression effects.

PA RAMPING CONTROLLER

The PA ramping controller of the ADF7242 minimises spectral splatter generated by the transmitter. Upon entering TX state the ramping controller automatically ramps the output power of the PA from the minimum output power to the specified nominal value. Transmission of the packet commences after the ramping phase. When the transmission of the telegram is complete or the TX state is left, the PA is turned off immediately.

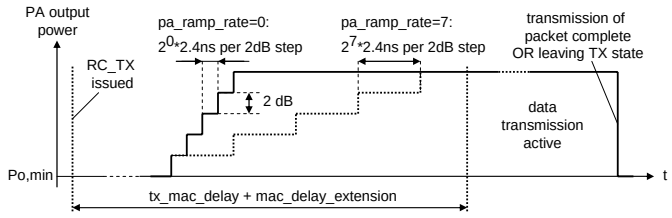


Figure 19: PA ramping profile

Figure 19 illustrates the shape of the PA ramping profile and its timing. It follows a linear-in-dB shape. The nominal output power of the PA is configured with register extpa_msc.pa_pwr. The ramp rate is specified with register pa_rr.pa_ramp_rate according to the equation

$$t\_ramp = 2^{pa\_rr.pa\_ramp\_rate} \cdot 2.4ns \cdot extpa\_msc.pa\_pwr$$

The ramp rate is irrespective of the output power setting and hence the ramp time depends on extpa_msc.pa_pwr.

EXTERNAL PA INTERFACE

The ADF7242 has an integrated biasing block for external PA circuits. It is especially suitable for external PA circuits based on a single GaAs MOSFET, and a wide range of integrated PA modules. The key elements are a switch between pins VDDBAT and PAVSUP, a 5 bit DAC and a bias servo loop, all of which are controlled by control logic.

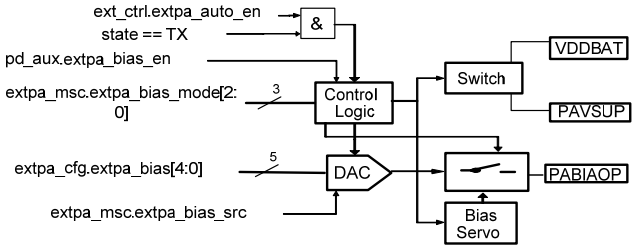


Figure 20: External PA interface

This interface is enabled either under direct control of the MCU by setting pd_aux.extpa_bias_en=1 while ext_ctrl.extpa_auto_en=0, or automatically while the ADF7242 is in TX state. Automatic mode is enabled by setting ext_ctrl.extpa_auto_en=1. When ext_ctrl.extpa_auto_en=1 the MCU should not alter the configuration of pd_aux.extpa_bias_en.

The reference current source for the DAC is controlled with extpa_msc.extpa_bias_src. If extpa_msc.extpa_bias_src=0 the current is derived from the external bias resistor. If extpa_msc.extpa_bias_src=1 the current is derived from the internal reference generator. The first option is more accurate and is recommended whenever possible.

The function of the two pins PAVSUP and PABIAOP depend on mode selected with extpa_msc.extpa_bias_mode as shown in Table 11.

Mode Options:

Mode 0: Allows supply to an external circuit to be switched on or off. This is useful for circuits which have no dedicated power down pin and or have a high power-down current.

Mode 1: Allows supply to an external circuit to be switched on or off. In addition the PABIOP pin acts as a programmable current source. A programmable voltage may be generated if a suitable resistor is connected between PABIAOP and GND.

Mode 2: Allows supply to an external circuit to be switched on or off. In addition the PABIOP pin acts as a programmable current sink. A programmable voltage may be generated if a suitable resistor is connected between PABIAOP and VDDBAT.

Mode 3: Same as mode 1, except that the switch between PAVSUP and VDDBAT is open, and the PAVSUP pin can be used for a different purpose.

Mode 4: Same as mode 2, except that the switch between PAVSUP and VDDBAT is open, and the PAVSUP pin can be used for a different purpose.

Mode 5: Intended for a PA circuit based on a single external FET. The supply voltage is controlled through the PAVSUP pin in order to ensure a low leakage current in power down state. The bias servo controls the gate bias voltage of the external FET such that the current through the supply switch is equal to a reference current. The reference current for bias servo is generated by the current DAC. In this mode, the bias servo expects the current in the FET to increase with increasing voltage at the PABIAOP output.

Mode 6: Same as mode 5 except that the bias servo expects the current in the FET to increase with decreasing voltage at the PABIAOP output.

Table 11: PA Interface

extpa_msc. extpa_bias_ mode	pd_aux. extpa_bias _en[1]	VDDBAT to PAVSUP switch	Function of pin PABIAOP
x	0	open	
0	1	closed	Not used
1	1	closed	Current source
2	1	closed	Current sink
3	1	open	Current source
4	1	open	Current sink
5	1	closed	Bias current servo output, positive polarity
6	1	closed	Bias current servo output, negative polarity
7	1	reserved	Reserved

Note [1] auto enabled when ext_ctrl.extpa_auto_en=1

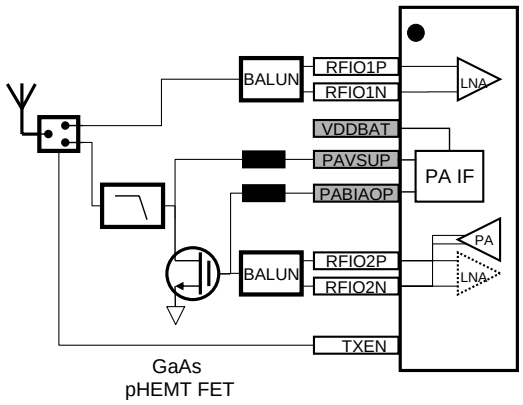


Figure 21. Typical External PA applications circuit

RF PORT CONFIGURATIONS/ ANTENNA DIVERSITY

ADF7242 is equipped with two fully differential RF ports. Port 1 is capable of receiving while port 2 is capable of receiving or transmitting. RF port 1 is comprised of pins RFIO1P and RFIO1N, RF port 2 is comprised of pins RFIO2P and RFIO2N. Only one of the two RF ports can be active at any one time.

The availability of two RF ports facilitates the use of switched antenna diversity and results in a simplified application circuit if the ADF7242 is connected to an external LNA and/or PA. Port selection for receive operation is configured through register rxfe_cfg.lna_sel.

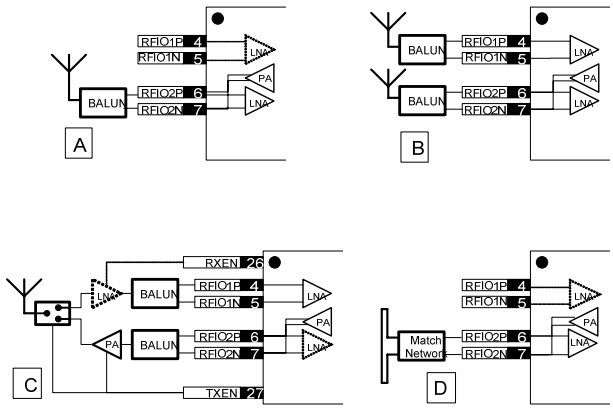


Figure 22.RF interface configuration options (A: single antenna; B: antenna diversity; C: external LNA/PA; D: dipole antenna)

Configuration A: Single antenna connected to RF port 2. This selection is made by setting pa_cfg.pa_controller_en=2 and rxfe_cfg.lna_sel=1.

Configuration B: Dual antenna configuration suitable for switched antenna diversity. For receive antenna diversity the link margin is maximised by selecting the optimum antenna based on the RSSI level of the desired signal received with each antenna. As an additional parameter the measured link quality may be considered (lrb.lqi_readback).

Suitable algorithms for the selection of the optimum antenna depend on the particulars of the underlying communication system. Switching between antennae is likely to cause a short interruption of the received data stream. Hence it is advisable to synchronise the antenna selection phase with the packet timing. In a static communication system it is often sufficient to select the optimum antenna once during setup.

Configuration C: Connecting an external PA and/or LNA is possible with a single external RX/TX switch. The PA is configured to transmit on RF port 2 (pa_cfg.pa_controller_en =2). RF port 1 is configured as the receive input (rxfe_cfg.lna_sel=0).

ADF7242 provides two signals, RXEN and TXEN to automatically enable an external LNA and/or a PA. TXEN and RXEN outputs are enabled by setting ext_ctrl.txen_en=1 and ext_ctrl.rxen_en=1, respectively. TXEN and RXEN signals have positive polarity. The ADF7242 outputs a logic HI level at the TXEN pin while in TX state and a logic LO level while in any other state. The same rules apply for the RXEN pin while RX state is active.

The RXEN and TXEN outputs have high impedance in SLEEP state. Hence appropriate pull-down resistors must be provided to define the correct state of these signals during power down. Refer to section on External PA Interface for further details on use of an external PA.

Configuration D: similar to configuration A, except that a dipole antenna is used. In this case a balun is not required.

RECEIVER

Rx operating Modes

The ADF7242 is capable of receiving IEEE 802.15.4-2.4 GHz compliant signals, as well as GFSK/FSK signals with bitrates specified in Table 10. It is recommended, but not required to operate the receiver with the modulation properties given in Table 10. The packet format and operating mode is configured with register rc_cfg.rc_mode. The choice is between an IEEE 802.15.4 compliant mode with packet handler support, a continuous IEEE 802.15.4 SPORT mode, and a GFSK/FSK SPORT mode. The SPORT modes are explained in more detail in section SPORT Interface.

The data rate is set with registers dr0.data_rate_high and dr1.data_rate_low as documented in the register map. It must be set to 2000 kbps in IEEE 802.15.4 mode, which is the default value.

IEEE802.15.4 RX TIMING AND CONTROL

The IEEE802.15.4 operating mode is configured with rc_cfg.rc_mode=0 for packet mode, and rc_cfg.rc_mode=2 for IEEE802.15.4 Rx SPORT mode. Please see section SPORT Interface for details on the operation of the SPORT interface. By default ADF7242 performs a synthesizer and an RX path calibration immediately after it has received an RC_RX command. The transition into RX state occurs after the Rx MAC delay has elapsed. The total Rx MAC delay is determined by the sum of the delay times configured in registers delay_cfg0.rx_mac_delay and delay_cfg2.mac_delay_ext. Both registers are programmable in steps of 1 µs. For IEEE802.15.4 Rx operation the parameter delay_cfg2.mac_delay_ext is typically set to 0. It can however be dynamically used to accurately align the Rx slot timing. If the programmed delay time is shorter than the RX path calibration time, the radio controller enters RX state immediately after the RX path calibration has been completed.

The transition into RX state enables the search for a valid SFD (IEEE 802.15.4 mode). Any data prior the state change is ignored. If enabled, the transition also causes the assertion of an rc_ready interrupt.

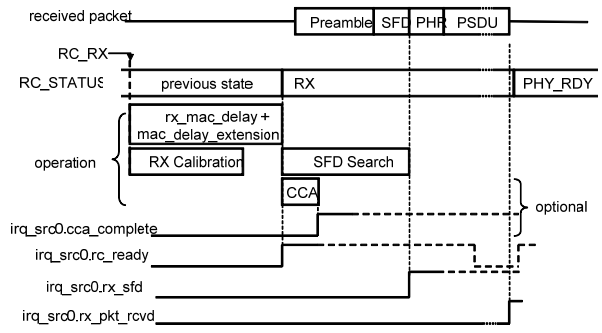


Figure 23: Rx Timing and Control (IEEE 802.15.4 mode)

When cca_cfg1.rx_auto_cca=1 a CCA measurement is started at the same time. The radio controller asserts a cca_complete interrupt once the CCA result is available in the status word. Upon detection of the SFD or sync word, the radio controller asserts an rx_sfd interrupt, which may be used by the MCU for synchronization purposes. Per default the ADF7242 transitions into state PHY_RDY once a valid frame has been received into the RX_BUFFER and if enabled an rx_pkt_rcvd interrupt is asserted. This mechanism protects the integrity of the RX_BUFFER. The RX state may be exited at any time by means of an appropriate radio controller command.

Figure 23 shows the timing sequence for IEEE802.15.4 packet mode (rc_cfg.rc_mode=0). The only difference between the timing sequence for IEEE 802.15.4 packet mode (rc_cfg.rc_mode=0), and IEEE 802.15.4 continuous mode (rc_cfg.rc_mode=2) is that no rx_pkt_rcvd interrupt is generated and no automatic transition into state PHY_RDY occurs in rc_cfg.rc_mode=2.

GFSK/FSK RX TIMING AND CONTROL

GFSK/FSK Rx mode is enabled by setting rc_cfg.rc_mode=3. Please see section SPORT Interface for details on the operation of the SPORT interface. Figure 24 shows the timing and control sequence for GFSK/FSK mode. Although similar, there are a few differences in comparison to the IEEE802.15.4 mode.

In order to accommodate the longer channel offset voltage acquisition time required for GFSK/FSK reception, the total Rx MAC delay must be set to 320 µs. Assuming that parameter delaycfg0.rx_mac_delay remains at the default delay setting of 192 µs this requires parameter delaycfg1.mac_delay_ext to be set to 128 µs. Optimal receiver performance is achieved when no input signal is present during the Rx MAC delay.

Following the Rx MAC delay, the transceiver enters the RX state. Depending on the setting of register gp_cfg.gpio_config the transceiver starts to search for a valid preamble/sync word combination or starts to output data on the SPORT interface immediately. Please refer to section SPORT Interface for details.

When enabled an rx_sfd interrupt is asserted when a preamble followed by the correct sync word has been received. Please note however that the framing signal appearing on the IRQ2_TRFS_GP2 output is more timing accurate than the rx_sfd interrupt. In GFSK/FSK SPORT mode no rx_pkt_rcvd interrupt is generated, and a command to enter an alternative state must be issued in order to exit the RX state.

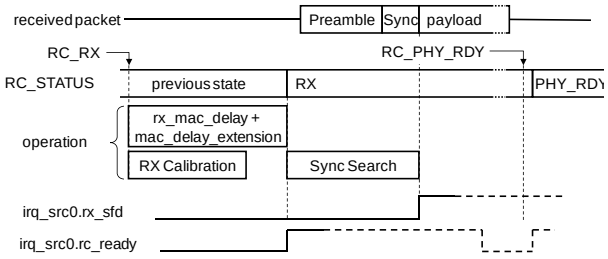


Figure 24: Rx Timing and Control (GFSK/FSK mode)

RX GFSK/FSK DEMODULATOR

Figure 25 shows a block diagram of the Rx demodulator. The correlator demodulator must be configured with register dm_cfg0.discriminator_bw to match the deviation frequency of the received signal. For applications with low data rates, the frequency error between the local oscillator of the transmitter and receiver can be a significant fraction of the deviation frequency. This frequency error must be considered when optimizing the demodulator setting in order to ensure reliable operation. Please refer to the register map for recommended settings for register dm_cfg0.discriminator_bw. For GFSK/FSK mode AFC may be used to improve frequency error tolerance.

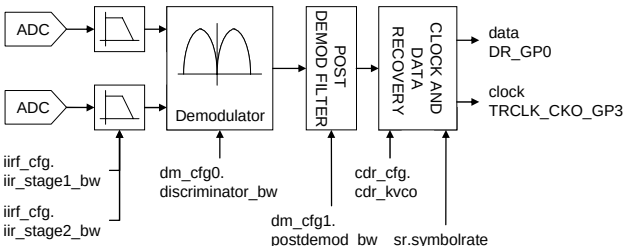


Figure 25: Structure of Rx demodulator

The digital post demodulator filter removes excess noise from the demodulator output. Its bandwidth is programmable with register dm_cfg1.postdemod and must be optimized for a particular data rate. If the bandwidth is set too narrow, performance degrades due to intersymbol interference. If the bandwidth is set too wide, performance degrades due to excess noise. The register map lists settings for the recommended modulation formats.

An oversampled digital clock and data recovery (CDR) PLL is used to resynchronize the received bit stream to a local clock. The data rate of the CDR must be configured with register dr.data_rate. The gain of the CDR PLL is set with register cdr_cfg.cdr_kvco. The register map lists settings for the recommended modulation formats. The maximum data rate tolerance of the CDR depends on the number of data transitions in the received packet. A maximum tolerance of tbd ppm is achieved for a 101010 preamble. This tolerance is reduced during the recovery of the remainder of the packet where data transitions may not occur on regular intervals. To maximize the data rate tolerance of the CDR, some form of encoding and/or data scrambling is recommended, so that a number of transitions are guaranteed at regular intervals.

The CDR is designed for fast acquisition of the recovered symbols during the preamble and typically achieves bit synchronization within five symbol transitions.

RX PATH CALIBRATION

The RX path is calibrated each time an RC_RX command is issued. The sequence is identical for IEEE802.15.4 and GFSK/FSK mode of operation; the timing parameters however are different. Figure 26 outlines the synthesizer and RX path calibration sequence and timing for the IEEE802.15.4 mode of operation. Figure 27 shows the same for GFSK/FSK mode of operation.

The calibration step VCO_cal is omitted by setting cal_cfg.vco_cal_cfg=3, which is an option if the value of ch_freq[23:0] remains unchanged during transitions between states PHY_RDY, RX or TX. The PLL settling phase is always required since the PLL bandwidth changes between Rx and Tx operation. The static offset correction phase (OCL_stat) and dynamic offset correction phase (OCL_dyn) are also mandatory.

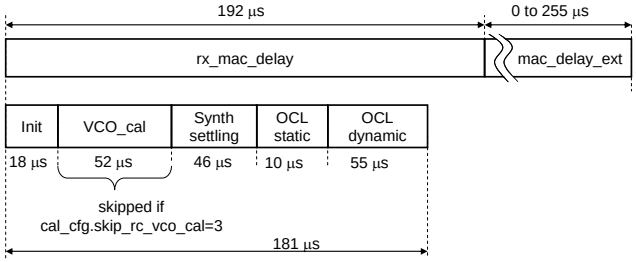


Figure 26: RX path calibration, IEEE802.15.4 mode

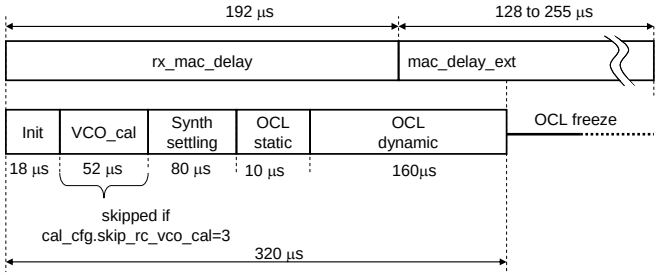


Figure 27: RX path calibration, GFSK/FSK mode

BASEBAND FILTER

The bandwidth of the analog baseband filter is programmable from 600 kHz to 1500 kHz in 100 kHz steps through register rxfe_cfg.rxbb_bw_ana. The bandwidth of the digital filter may be set with registers iirf_cfg.iir_stage1_bw and

iirf_cfg.iir_stage2_bw. The recommended settings for the analog and digital filter stage shown in the register map are based on the modulation parameters shown in Table 10 assuming a crystal frequency tolerance of +/-20 ppm for GFSK/FSK and +/-40 ppm for IEEE 802.15.4 mode. Depending on the application an optimization of the filter parameters may help to improve the receiver performance. Any changes of register rxfe_cfg.rxbb_bw_ana only take effect on transition from IDLE to PHY_RDY state.

AGC

The ADF7242 AGC circuit features fast overload recovery and sliding bandwidth averaging for fast preamble acquisition and optimum utilization of the dynamic range of the receive path.

The radio controller automatically enables the AGC when the transceiver enters RX state. The optimum configuration parameters depend on the selected datarate, the modulation format, and the configuration of the RX path offset correction loop. The register map documents recommended settings for all AGC configuration registers based on the modulation parameters shown in Table 10.

Status bit agcstat.agc_settled may be read back to determine if the AGC has settled or is in a transient state. Configuration bit agc_cfg1.agc_lock may be used to freeze the AGC after the reception of the packet header for the duration of the remainder of the packet.

OCL (OFFSET CORRECTION LOOP)

The ADF7242 is equipped with an offset correction loop (OCL), which operates differently in IEEE802.15.4 and GFSK/FSK mode. In the IEEE802.15.4 modes (rc_cfg.rc_mode=0 and rc_cfg.rc_mode=2) the OCL operates in a continuous fashion and is not constrained by any packet timing or synchronization requirements. In GFSK/FSK mode (rc_cfg.rc_mode=3) the OCL is active only during the Rx path calibration. After acquiring the offset voltage in the Rx path, the OCL is frozen until the next RC_RX command is issued. This scheme is well suited for FHSS communication system and allows the ADF7242 to maintain full sensitivity independent of packet formatting constraints. However, since the offset voltages in the Rx path are subject to drift, it imposes an upper limit on the channel dwell time. When operating in GFSK/FSK mode, it is recommended to re-issue the RC_RX command at least every 400ms.

Default settings for the different operating modes are listed in the register map (registers ocl_bw0, ocl_bw1, ocl_bw2, ocl_bw3, ocl_bw4, ocl_bws, ocl_cfg1, ocl_cfg13).

RSSI

The RSSI readback value is continuously updated while the ADF7242 is in RX state. The result is provided in register rrb.rssi_readback in dBm using signed 2's compliment notation. The RSSI averaging window is synchronized with the start of the active RX phase at the end of the rx_mac_delay following an RC_RX command. The RSSI averaging time is programmable with register agc_cfg5.rssi_avg_time, and depends on the AGC update rate according to the following dependency:

T_avg_rssi = 77ns * 2 ^ (2 + agc_cfg5.agc_filt1_tavg + agc_cfg6.agc_filt2_tavg2 + agc_cfg5.rssi_avg_time)

In IEEE 802.15.4 mode the default RSSI averaging period of 128 µs, or 8 symbol periods must be used for compliance. If the ADF7242 is operating in IEEE 802.15.4 packet mode (rc_cfg.rc_mode=0), and pkt_cfg.auto_fcs_off=0, the RSSI of received frames is measured and stored together with the frame in the RX_BUFFER. The RSSI is measured in a window with a length of 8 symbols immediately following the SFD. The results are then stored in place of the first byte of the FCS of the received frame in the RX_BUFFER.

For GFSK/FSK the optimum RSSI averaging time is application dependent. The default settings should be appropriate for most applications.

It is possible to compensate systematic errors of the measured RSSI value and/or production tolerances through adjusting the RSSI offset value in register agc_cfg5.rssi_offs in one decibel steps.

CCA

The CCA function of the ADF7242 complies with CCA Mode 1 as per IEEE 802.15.4. It is also applicable for GFSK/FSK mode of operation.

A CCA can be specifically requested by means of an RC_CCA command or automatically obtained when the transceiver enters the RX state. In both cases the start of the CCA averaging window is defined by the instant the RC_CCA or RC_RX command is issued and the delay configured in registers delaycfg0.rx_mac_delay and delaycfg2.mac_delay_ext. The CCA result is determined by comparing cca1.cca_thres against the average RSSI value measured throughout the CCA averaging window. If the measured RSSI value is less than the threshold value configured in cca.cca_thres, then the CCA_RESULT bit in the status word is set, otherwise it is reset. The cca_complete interrupt is asserted when the CCA_RESULT bit in the status word is valid.

Figure 28 shows the timing sequence of the RC_CCA controlled CCA request when configuration bit cca2.continuous_cca=0. Following the RC_CCA command the transceiver starts the CCA observation window after the delay specified by the sum of delaycfg0.rx_mac_delay and delaycfg2.mac_delay_ext has elapsed. The restrictions and conventions outlined in section IEEE802.15.4 Tx Timing and Control or GFSK/FSK Tx Timing and Control fully apply. A cca_complete interrupt is asserted at the end of the CCA averaging window and the transceiver enters PHY_RDY state.

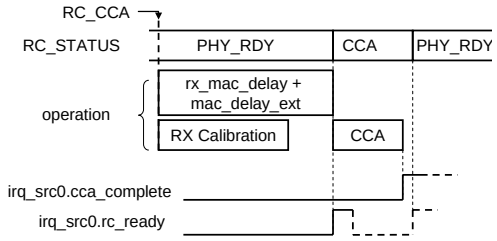


Figure 28: CCA timing sequence, cca2.continuous_cca=0

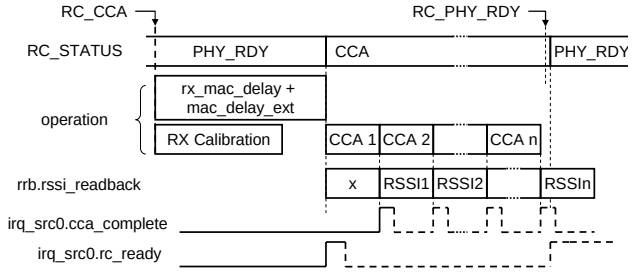


Figure 29: CCA timing sequence, cca2.continuous_cca=1

When configuration bit cca2.continuous_cca=1, the transceiver remains in CCA state and continues to calculate CCA results repeatedly until a RC_PHY_RDY command is issued. This case is illustrated in Figure 29. The first cca_complete interrupt occurs when the first CCA averaging window after the Rx MAC delay has elapsed. The transceiver then repeatedly restarts the CCA averaging window each time a cca_complete interrupt is asserted. This configuration is useful for longer channel scans, either by immediately evaluating the CCA_RESULT bit to identify if the configured CCA RSSI threshold value has been exceeded during a CCA averaging period, or by reading the RSSI value rrb.rssi_readback value after each cca_complete interrupt and processing the value in the user MCU. As indicated in Figure 29 the RSSI readback value in the rrb.rssi_readback register holds the results of the previous RSSI measurement cycle throughout the CCA averaging window and is updated only shortly before the cca_complete interrupt is asserted.

The RSSI averaging time is programmable with register agc_cfg5.rssi_avg_time according to Table 12. While operating the transceiver in IEEE802.15.4 mode, setting agc_cfg5.rssi_avg_time=2 is required for compatibility.

Table 12: RSSI averaging time

agc_cfg5.rssi_avg_time	CCA averaging period
0	32us
1	64us
2	128 us
3	256us

LINK QUALITY INDICATION

The link quality indication (LQI) is defined in the IEEE 802.15.4 standard as a measure of the signal strength and signal quality of a received IEEE 802.15.4 frame. The ADF7242 makes several measurements available from which an IEEE 802.15.4 compliant LQI value can be calculated in the MCU. The first parameter is the RSSI value, which has been discussed previously.

The second parameter required for the LQI calculation may be read from register lrb.lqi_readback, which contains an 8-bit value representing the quality of a received IEEE 802.15.4 frame. It increases monotonically with the signal quality, and must be scaled to comply with the IEEE 802.15.4 standard.

If the ADF7242 is operating in IEEE 802.15.4 packet mode (rc_cfg.rc_mode=0), and pkt_cfg.auto_fcs_off=0, the LQI of a received frame is measured and stored together with the frame in the RX_BUFFER. The LQI is measured immediately following the SFD, and stored in place of the second byte of the FCS of the received frame in the RX_BUFFER.

GFSK SYNC WORD AND PREAMBLE

In GFSK/FSK mode (rc_cfg.rc_mode=3) the ADF7242 supports automatic detection of a sync word or ID field with a length of up to 24 bits and up to 3 bit tolerated mismatches. This feature can be used to alert the MCU that a valid sync word has been detected, which relaxes computational requirements and hence the overall power consumption.

When rc_cfg.rc_mode=3, the output bit stream in SPORT mode is gated with the sync word match signal. Any data output prior to detection of a sync match is inhibited. The data output commences with the first bit following the sync word, which can relax computational overhead in some MCUs and DSPs.

To activate sync word detection, field sync_word[23:0] must be programmed in registers sync_w0, sync_w1, and sync_w2. The length of the sync word is then configured in register sync_cfg.sync_len. During the comparison the MSB is always considered first. Sync word detection is disabled if sync_cfg.sync_len=0. An error tolerance parameter can be programmed in register sync_cfg.sync_tol that accepts a valid match when up to 3 bits of the word are incorrect. An rx_sfd interrupt is raised on detection of a match with the synchronization word. Please note that update of variables sync_word[23:0], sync_len or sync_tol only takes effect after a RC_RX command.

The ADF7242 sync word detection algorithm first searches for a valid preamble sequence. A '01' pattern must be used for the preamble. Once at least 24 valid preamble bits have been received the ADF7242 starts to search for the actual sync word. However, it must be considered that the preamble is not received correctly while the AGC acquires the signal. When using the AGC parameters given in the register map, an AGC

acquisition of typically 25 µs is achieved. Hence for GFSK at 2 Mbps for example, at least 50 preamble bits are required to achieve correct signal acquisition. Therefore for 2 Mbps at least 50+24=74 preamble bits are required for correct operation of the sync word detection feature. For GFSK at 62.5 kbps on the other hand, the symbol period is 16 µs and hence only 2 preamble bit are required for correct signal acquisition. In this case a minimum of 2+24=26 preamble bits are required.

AFC

The ADF7242 is equipped with a fully automatic real-time AFC function. It is used to maintain an optimal link budget in the presence of frequency errors between the local oscillators of receiver and transmitter. AFC is operational in GFSK/FSK mode only. The AFC circuit monitors the frequency error of the received signal at the output of the FSK discriminator. The frequency of the synthesizer is adjusted based on the measured frequency error by a proportional-integral (PI) control loop.

Setting afc_cfg.afc_mode=3 enables AFC operation with automatic preamble locking. The frequency correction is active until 35 valid preamble bits have been detected in the received bitstream. Subsequently the AFC loop is locked and freezes the correction value determined during the preamble phase. The lock remains active until the next RC_RX command is issued. The frequency error readback word in register afc_read.afc_freq_error is continuously updated while the AFC is locked.

The settings for the control loop parameters afc_ki_kp.afc_ki and afc_ki_kp.afc_kp are dependent on the datarate. Optimal values for each datarate are listed in the register map. The bandwidth of the closed-loop transfer function of the AFC loop and hence the AFC settling time is weakly dependent on the datarate. While the fastest AFC settling time occurs at the highest datarate, the lowest number of preamble bits required for complete AFC settling occurs at the lowest datarate. As a simple rule 32 valid preamble bits are required for AFC settling under worst case conditions irrespective of the selected datarate. This allows the calculation of the minimum number of preamble bits when using AFC. The calculation must consider the AGC acquisition time, which is typically 25 µs irrespective of the datarate. At 2 Mbps, a preamble of at least ceiling (25 µs / 0.5 µs + 32) bits = 82 bits is required. At 62.5 kbps this reduces to ceiling (25 µs / 16 µs + 32) bits = 34 bits.

The maximum correction range is programmable in 1 kHz steps with register afc_range.max_afc_range. The maximum AFC correction range is the frequency difference between the upper and lower limit of the AFC tuning range. This range is centered symmetrically around the nominal synthesizer frequency set with the frequency control word ch_freq[23:0].

The adjacent channel rejection (ACR) performance of the receiver can be degraded when AFC is enabled and the AFC correction range is close to twice the effective baseband bandwidth configured with registers rxfe_cfg.rxbb_bw_ana, iirf_cfg.iir_stage1_bw and iirf_cfg.iir_stage2_bw. The setting of register afc_range.max_afc_range can be optimised to find the best trade-off between correction range and ACR.

IEEE802.15.4 non standard SFD

An alternative to the standard IEEE 802.15.4 SFD byte may optionally be selected by the user. The default setting of register sfd_15_4.sfd_symbol_1/sfd_symbol_2 is the standard IEEE 802.15.4 SFD. If the user programs this register with an alternative value, this will be used as the SFD in receive and transmit in IEEE 802.15.4 mode.

IEEE 802.15.4 RX PACKET MODE

IEEE 802.15.4 mode with paket handling support is selected when rc_cfg.rc_mode=0. The RX_BUFFER will be overwritten when the ADF7242 has entered RX state following an RC_RX command and an SFD is detected. The SFD is stripped off the incoming frame, and all data following and including the frame length (PHR) is written to the RX_BUFFER.

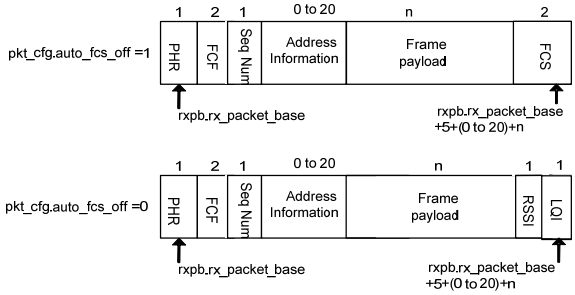


Figure 30: Data written to RX_BUFFER

If pkt_auto_fcs_off=1, then the FCS of the incoming frame is stored in the RX_BUFFER. Once the entire frame has been received an rx_pkt_rcvd interrupt is asserted irrespective of the correctness of the FCS. If pkt_auto_fcs_off=0, the radio controller calculates the FCS of the incoming frame according to the FCS polynominal defined in the IEEE 802.15.4 standard,

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

and compares the result against the FCS of the incoming frame. An rx_pkt_rcvd interrupt is asserted only if both FCS fields match. The FCS is not written to the RX_BUFFER, but replaced with the measured RSSI and LQI values of the received frame.

The behavior of the radio controller following the reception of a frame may be configured with buffercfg.rx_buffer_mode. With the default setting buffercfg.rx_buffer_mode=0, the part reverts automatically to PHY_RDY once an rx_pkt_rcvd interrupt condition occurs. Since a new frame is always written to the RX_BUFFER starting from address rxpb.rx_packet_base, this mode prevents the RX_BUFFER being overwritten by the next

frame prior to the MCU having read it from the ADF7242. Please note that reception of the next frame is inhibited until the Rx synchronization delay following an RC_RX command has elapsed.

If buffercfg.rx_buffer_mode=1, the part remains in RX state and the reception of the next packet is enabled a MAC delay period after frame has been written to the RX_BUFFER. Depending on the network setup, this mode can cause an unnoticed violation of the RX_BUFFER integrity, should a frame arrive prior to the MCU having read the frame from the RX_BUFFER.

If buffercfg.rx_buffer_mode=2, the reception of frames is disabled. This mode is useful for RSSI measurements and CCA, if the contents of the RX_BUFFER are to be preserved.

IEEE802.15.4 AUTO RX TURNAROUND MODE

The ADF7242 features an automatic Tx to Rx turnaround mode when operating in IEEE 802.15.4 packet mode (rc_cfg.rc_mode=0). The automatic Rx turnaround mode facilitates the timely reception of acknowledgement frames.

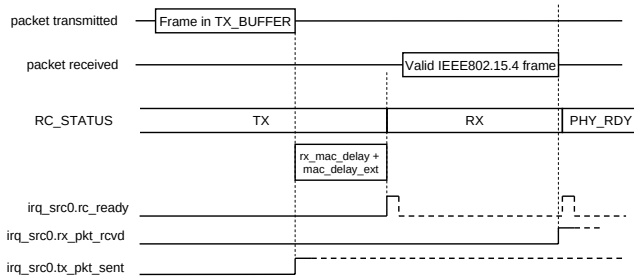


Figure 31: Auto Rx Turnaround Mode

Figure 31 illustrates the timing of the automatic Rx turnaround mode. When enabled by setting register bit buffer_cfg.auto_rx_turnaround the ADF7242 automatically enters RX state following the transmission of an IEEE802.15.4 frame. After the combined Rx MAC delay (rx_mac_delay + mac_delay_ext) the ADF7242 enters RX state and is ready to receive a frame into the RX_BUFFER. Subsequently once a valid IEEE802.15.4 frame has been received, the ADF7242 enters PHY_RDY state. Apart from the automatic transition the normal functionality of the RX and TX states is available.

BATTERY MONITOR

The battery monitor features very low power consumption and may be used in parallel with any mode of operation, except SLEEP state. The battery monitor generates a batt_alert interrupt for the MCU when the battery voltage drops below the programmed threshold voltage. The default threshold voltage is 1.7 V, and can be increased in 62 mV steps to 3.6 V with register bm_cfg.battmon_voltage. In order to avoid the repetitive generation of IRQ conditions the threshold setting in register bm_cfg.battmon_voltage may be increased once the battery alert condition has occurred for the first time.

AUXILLARY FUNCTIONS

Temp Sensor

To perform a temperature measurement the MEAS state is invoked using command RC_MEAS. The result may be read back from register adc_rbk.adc_out.
The die (ambient) temperature is calculated as follows:

$$teta = -174.6\ °C + 4.05\ °C \cdot adc\_rbk.adc\_out$$

INTERFACE

SERIAL CONTROL INTERFACE

General Characteristics

The ADF7242 is equipped with a 4 wire SPI interface, using pins SCLK, SO, SI and CSN. The ADF7242 always acts as a slave. Figure 32 shows an example connection diagram between MCU and ADF7242. The diagram also shows the direction of the signal flow for each pin. The SPI interface is active and the SO output enabled only while the CSN input is low. The interface uses a word length of 8 bits, which is compatible with the SPI hardware of most MCUs. The data transfer through the SPI interface occurs with the most significant bit first. The SI input is sampled at the rising edge of SCLK. As commands or data is shifted in from the SI input at the SCLK rising edge, the status word or data is shifted out at the SO pin synchronous with the SCLK clock falling edge. If CSN is brought low, the MSB of the status word appears on the SO output without the need for a rising clock edge on the SCLK input.

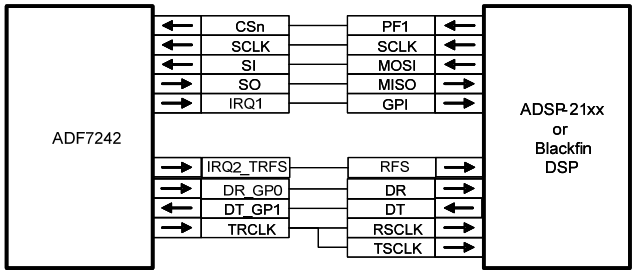


Figure 32. SPI interface connection

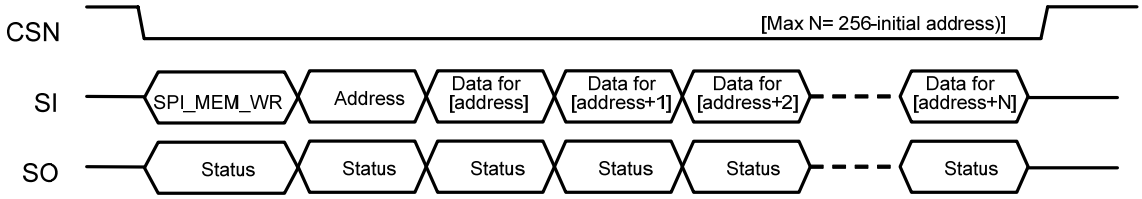


Figure 33: Memory (register or Packet RAM) Block Write

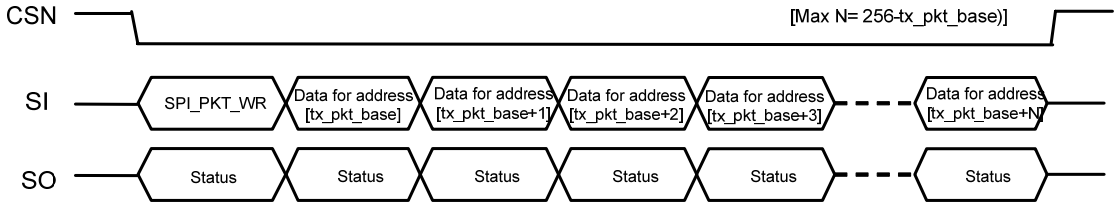


Figure 34: Packet RAM Write

Note: tx_pkt_base is address base pointer value for Tx which is programmed in register **txbp.tx_pkt_base**

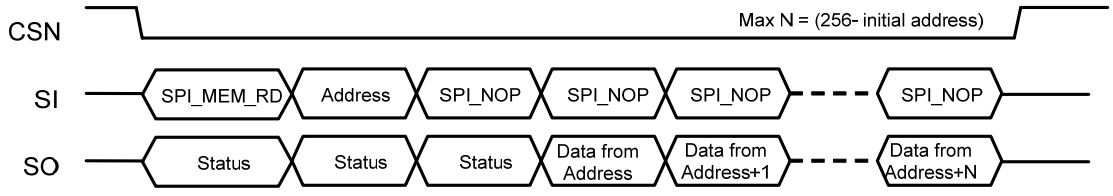


Figure 35: Memory (register or Packet RAM) Block Read

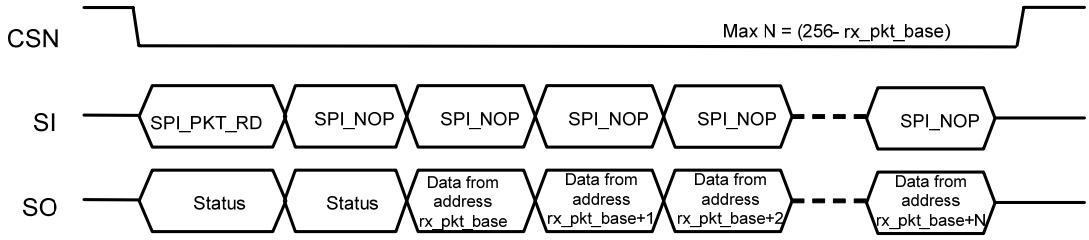


Figure 36: Packet RAM Read

Note: rx_pkt_base is address base pointer value for Rx which is programmed in register rxbp.rx_pkt_base

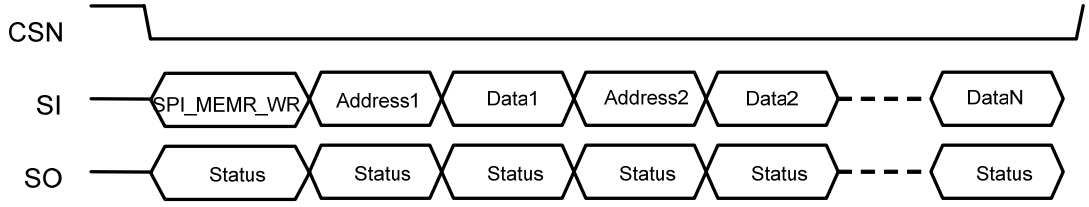


Figure 37: Memory (register or Packet RAM) Random Address Write

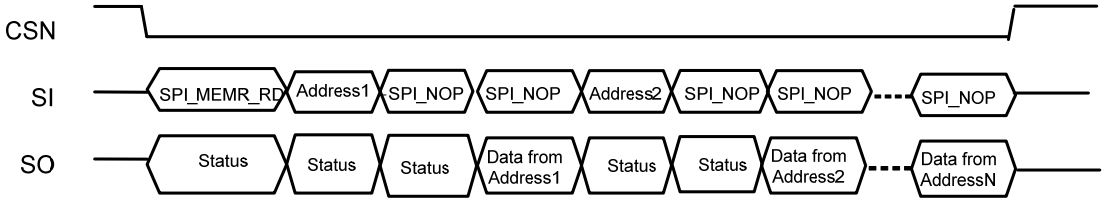


Figure 38: Memory (register or Packet RAM) Random Address Read

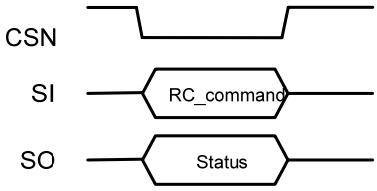


Figure 39: Command write

Wake-up from SLEEP state

The MCU can bring CSN low at any time in order to wake the ADF7242 from SLEEP state. After bringing CSN low, it must wait until the SO output (spi_ready flag) goes high prior to accessing the SPI port. This delay reflects the start-up time of the ADF7242. Once the SO output is high, the voltage regulator of the digital section and the crystal oscillator have stabilized. Unless the chip was in SLEEP state, the SO pin will always go high immediately after taking CSN low.

Command Access

The ADF7242 is controlled through commands. Command words are single byte instructions, which control the state transitions of the radio controller and access to the Registers and Packet RAM. The complete list of valid commands is given in Table 13. Commands with the RC prefix are handled by the radio-controller, whereas commands with the SPI prefix are handled independently. Thus SPI commands can be issued independent of the state of the radio controller.

A command is initiated by bringing CSN low and shifting in the command word. The CSN input must be brought high again once a command, including any parameters has been shifted into the ADF7242 in order to enable the recognition of successive command words (see Figure 39)

Table 13: Command list

Command	Code	Description
SPI_NOP	0xFF	No operation. Use for dummy writes.
SPI_PKT_WR	0x10	Write telegram to the Packet RAM starting from the TX packet base address pointer tx_packet_base
SPI_PKT_RD	0x30	Read telegram from the Packet RAM starting from RX packet base address pointer rxpb.rx_packet_base.
SPI_MEM_WR	0x18+reg_address[10:8]	Write data to MCR or Packet RAM sequentially.
SPI_MEM_RD	0x38+reg_address[10:8]	Read data from MCR or Packet RAM sequentially.
SPI_MEMR_WR	0x08+reg_address[10:8]	Write data to MCR or Packet RAM as random block.
SPI_MEMR_RD	0x28+reg_address[10:8]	Read data from MCR or Packet RAM as random block.
RC_SLEEP	0xB1	Invoke transition of radio controller into SLEEP state
RC_ IDLE	0xB2	Invoke transition of radio controller into IDLE state
RC_PHY_RDY	0xB3	Invoke transition of radio controller into PHY_RDY state
RC_RX	0xB4	Invoke transition of radio controller into RX state
RC_TX	0xB5	Invoke transition of radio controller into TX state
RC_MEAS	0xB6	Invoke transition of radio controller into MEAS state
RC_CCA	0xB7	Invoke Clear channel assessment

The execution of certain commands by the radio controller can take some time, during which the radio controller unit is busy. Prior to issuing a radio controller command it is therefore necessary to read the status word in order to determine if the ADF7242 is ready to accept a new radio controller command. This is best accomplished by shifting in SPI_NOP commands, which will cause the status words to be shifted out. In order to take the burden of repeatedly polling the status word off the MCU for complex commands such as RC_RX, RX_TX and RC_PHY_RDY, the IRQ handler can be configured to generate an rc_ready interrupt. Please refer to the section on interrupts for details. Otherwise the user may programme timeout periods according to the command execution times provided.

Status Word

The RC_STATUS field in the status word reflects the current state of the radio controller. The RC_STATUS value is identical to the contents of register rc_state. Per definition RC_STATUS reflects the state of a completed state transition. During the state transition RC_STATUS maintains the value of the state in which the state transition was invoked.

Table 14: SPI status word

bit field	Bit name	description
[7]	SPI_READY	0: SPI is not ready for access 1: SPI is ready for access
[6]	IRQ_STATUS	0: No pending interrupt condition 1: Pending interrupt condition (mirrors IRQ pin)
[5]	RC_READY	0: Radio controller is not ready to accept RC_xx command strobe 1: Radio controller is ready to accept new RC_xx command strobe
[4]	CCA_RESULT	0: Channel Busy, 1:Channel Idle Valid when irq_source0.cca_complete is asserted.
[3:0]	RC_STATUS	Radio controller status: 0: reserved 1: IDLE 2: MEAS 3: PHY_RDY 4: TX 5: RX 6..15: reserved

Memory Map

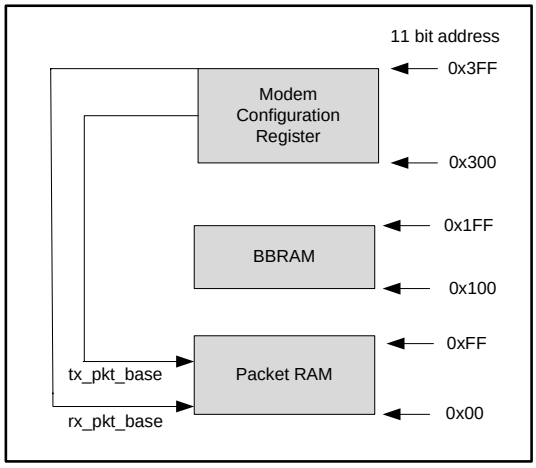


Figure 40. Memory Map

The ADF7242 contains three main blocks of memory. The BBRAM and MCR registers are programmed to configure the part. The BBRAM is used to maintain device configuration settings needed at wake up from sleep mode by the wake up timer. Contents of MCR and Packet RAM are reset during SLEEP state. The Packet RAM is used to hold received data and data to be transmitted. The value of register rxbp.rx_pkt_base determines the start address for storing received data. The value of register txpb.tx_pkt_base determines the start address of data to be transmitted.

Writing to the ADF7242

Registers may be written to by invoking the SPI_MEM_WR or SPI_MEMR_WR commands. An 11 bit address, reg_address[10:8] is used to identify registers or locations in ADF7242 memory space. The most significant 3 bits of the address, reg_address[10:8] are incorporated into the command by adding them to the LSBs of the command word. Thus for example if reg_address[10:8] =3 then the SPI_MEM_WR command is 0x18+reg_address[10:8] =0x1B. These commands are followed by the remaining 8 bits of the register address, reg_address[7:0] and the data to be written to it. In the case of SPI_MEM_WR if more than one data byte is written, the write address is automatically incremented for every byte sent until CSN =1 terminates the command. Figure 33 illustrates the access sequence for this command. In the case of SPI_MEMR_WR the lower 8 bits of the next address are entered followed by the data for that address until all required addresses within that block are written as shown in Figure 37.

Command SPI_PKT_WR provides pointer-based write access to the Packet RAM. The address of the location written to is calculated from the base address in txpb.tx_pkt_base plus an index. The index is zero for the first data word following the command word, and is auto-incremented for each consecutive data word written. The first data word following a SPI_PKT_WR command is thus stored in the location with the address txpb.tx_pkt_base, the second in Packet RAM location with address txpb.tx_pkt_base +1 and so forth. This feature makes this command efficient for bulk writes of data which recurrently begin at same address. Figure 34 shows the access sequence for command SPI_PKT_WR. It is also possible to access the Packet RAM with the SPI_MEM_WR and SPI_MEMR_WR commands, which facilitates the modification of individual elements of a packet in the Rx and TX_BUFFER without the need to download and upload an entire packet. The address location of a particular byte in the RX_BUFFER and TX_BUFFER in the Packet RAM is determined by adding the relative location of a byte to the address pointer rxpb.rx_base_pointer or txpb.tx_base_pointers, respectively.

Some configuration bits in the MCR are accessed by the radio controller during normal operation and are marked as RC_CONTROLLED in the register map. These registers should only be written to in IDLE state and RC_CONTROLLED bits should be set to their default values.

Reading from the ADF7242

Registers are read by invoking the SPI_MEM_RD or SPI_MEMR_RD command. The most significant 3 bits of the address, reg_address[10:8] to be read are incorporated into the command word. Thus for example if the 3 MSBs of the address to be read are reg_address[10:8] =3 then the SPI_MEM_RD command is 0x38+reg_address[10:8] =0x3B. These commands are followed by the remaining 8 bits of the address to read and then 2 dummy byte SPI_NOP commands. The first byte available after writing the address should be ignored, with the second byte constituting valid data. In the case of SPI_MEM_RD by shifting in additional dummy bytes the address of the location being read is automatically incremented. In the case of SPI_MEMR_RD the lower 8 bits of the next address within that memory block to be read should be entered followed by two dummy byte SPI_NOP commands. Again the first byte available after writing the address should be ignored, with the second byte constituting valid data. Figure 38 illustrates this command access sequence.

Command SPI_PKT_RD provides pointer based read access from the Packet RAM. The address of the location to be read is calculated from the base address in rxpb.rx_pkt_base plus an index. The index is zero for the first readback word. It is auto-incremented for each consecutive SPI_NOP command. The first data byte following a SPI_PKT_RD command is invalid and should be ignored. Figure 35 shows the access sequence for command SPI_PKT_RD.

It is also possible to read the Packet RAM using commands SPI_MEM_RD, and SPI_MEMR_RD. This allows individual elements of a packet in the RX_BUFFER and TX_BUFFER to

be read without the need to download the entire packet. The address location of a particular byte in the Rx and TX_BUFFER in the Packet RAM is determined by adding the relative location of a byte to the address pointer rxpb.rx_base_pointer or txpb.tx_base_pointers, respectively.

SPORT INTERFACE

The SPORT interface is a high speed synchronous serial interface suitable for interfacing to a wide variety of MCUs and DSPSs, especially the ADSP-21xx, SHARC, TigerSHARC and Blackfin DSPs without glue logic. **Figure 46** shows a typical application diagram. The interface uses 4 signals, a clock output (TRCLK_CKO_GP3), a receive data output (DR_GP0), a transmit data input (DT_GP1), and a framing signal output (IRQ2_TRFS_GP2). The IRQ2 output functionality is not available while the SPORT interface is enabled. The SPORT interface supports GFSK/FSK and IEEE802.15.4 receive and GFSK/FSK transmit operation. When using GFSK/FSK mode the polarity of the receive/transmit clock appearing on the TRCLK_CKO_GP3 output is programmable. A detailed overview of the function of the interface pins for each GFSK/FSK mode SPORT configuration is listed in Table 15. The corresponding list for IEEE802.15.4 mode is listed in Table 16. It is possible to use the SPORT interface for transmitting IEEE802.15.4 frames by configuring the ADF7242 in FSK-mode and providing the chipping sequence externally.

GFSK/FSK Transmit Operation

Figure 41 illustrates the operation of the SPORT interface in the transmit case. The SPORT interface is enabled by setting gp_cfg.gpio_config=1 or gp_cfg.gpio_config=4 depending on the desired clock polarity. Once enabled the data input of the transmitter is fully controlled by the SPORT interface. The transmit clock appears when the transmit MAC delay (tx_max_delay) has elapsed. The ADF7242 keeps transmitting the serial data presented at the DT_GP1 input until it is forced out of the TX state by means of a command. For IEEE 802.15.4 operation the ADF7242 should be configured for transmission with 2 Mbps MSK. A timing diagram is provided in Figure 9.

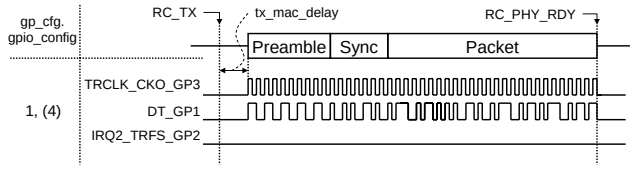


Figure 41: SPORT operation in TX state

GFSK/FSK Receive Operation

The SPORT interface supports GFSK/FSK receive operation with a number of modes to suit particular signaling requirements. For GFSK/FSK receive SPORT operation the packet format must be configured to rc_cfg.rc_mode =3, which disables any packet-level processing by the packet handler. The operating mode of the SPORT interface can be configured through register gp_cfg.gpio_config. Figure 42 shows an overview of all available configurations. SPORT configurations gp_cfg.gpio_config = 2, 3, 5, and 6 provide synchronization with a programmable sync word. For these modes, the synchronization block must be configured with registers sync_word0, sync_word1, sync_word2 and sync_config as outlined in section GFSK Sync Word prior to issuing command RC_RX.

Once the SPORT interface is providing output data either through successful packet synchronization or through forced synchronization (gp_cfg.gpio_cfg=1 or gp_cfg.gpio_cfg=4) data continues to appear on the interface pins until the RC_RX command is re-issued or the ADF7242 is forced out of the RX state by means of an appropriate SPI command. The following SPORT operating modes are selectable:

gp_cfg.gpio_config=1 or gp_cfg.gpio_config =4:

The data clock is enabled at the TRCLK_CKO_GP3 output together with the data signal at the DR_GP0 output during the RX MAC delay. The GFSK/FSK SYNC word is ignored in this configuration. The IRQ2_TRFS_GP2 output has no function. Figure 6 illustrates further timing details.

gp_cfg.gpio_config=2 or gp_cfg.gpio_config =5:

When a preamble signal has been detected the data clock and data signals start to appear at the TRCLK_CKO_GP3 and DR_GP0 output, respectively. The IRQ2_TRFS_GP2 output goes HIGH when the SYNC word has been detected in the received GFSK/FSK bit sequence. Figure 7 shows more timing details.

gp_cfg.gpio_config=3 or gp_cfg.gpio_config =6:

The data clock starts to appear at the TRCLK_CKO_GP3 output when a valid preamble and the SYNC word have both been detected in the received GFSK/FSK bit sequence. The first active clock edge corresponds with the first data bit following the GFSK/FSK SYNC word appearing on the DR_GP0 output. The framing signal IRQ2_TRFS_GP2 goes HIGH when the SYNC word has been detected in the received bit sequence. The DR_GP0 output signal is invalid prior to the first active clock edge appearing on the TRCLK_CKO_GP3 output. Figure 9 6 and 7 illustrate the applicable timing details.

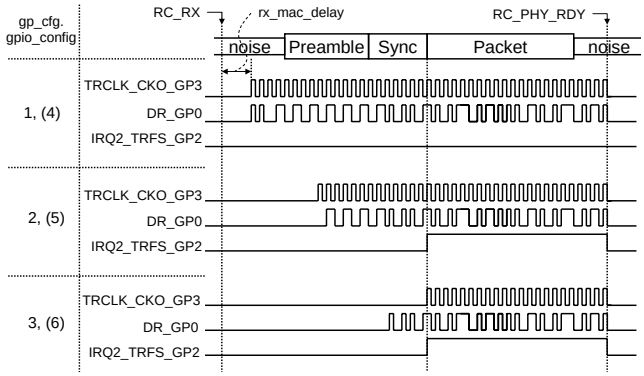


Figure 42: Overview of SPORT modes in RX state

Table 15: GFSK/FSK mode SPORT interface configurations

gp_cfg. gpio_cfg	IRQ2_TRFS_GP2	DR_GP0	DT_GP1	TRCLK_CKO_GP3
1	Rx mode : not used, low TX: not used, low	RX: data output, changes at falling edge of data clock TX: not used	RX: not used TX: data input, sampled at rising edge of data clock	RX: data clock TX: data clock
2	RX: goes high when sync match has been detected	RX: data output, changes at falling edge of data clock	RX: not used	RX: data clock, gated with detection of preamble
3	RX: goes high when sync match has been detected	RX: data output, changes at falling edge of data clock	RX: not used	RX: data clock, gated with detection of sync word
4	RX: not used, low TX: not used, low	RX: data output, changes at rising edge of data clock TX: not used	RX: not used TX: data input, sampled at falling edge of data clock	RX: data clock TX: data clock
5	RX: goes high when sync match has been detected	RX: data output, changes at rising edge of data clock	RX: not used	RX: data clock, gated with detection of preamble
6	RX: goes high when sync match has been detected	RX: data output, changes at rising edge of data clock	RX: not used	RX: data clock, gated with detection of sync word

Table 16: IEEE802.15.4 mode SPORT interface configuration

gp_cfg. gpio_cfg	IRQ2_TRFS_GP2	DR_GP0	DT_GP1	TRCLK_CKO_GP3
3	RX: not used	RX: data output, changes at rising edge of data clock	RX: not used	RX: data clock
7	RX: ignore	RX: ignore	RX: ignore	RX: symbol clock

IEEE 802.15.4 Rx SPORT Mode

The ADF7242 provides an IEEE802.15.4 compliant operating mode in which the SPORT interface is active and the packet handler is bypassed. It allows the reception of packets of arbitrary length. The mode is enabled by setting rc_cfg.rc_mode = 2 and gp_cfg.gpio_cfg=3. Once the SFD has been detected, data and clock signals appear on the SPORT outputs DR_GP0 and TRCLK_CKO_GP3, respectively. The SPORT bus remains active, until an RC_RX command is issued or the ADF7242 is forced to exit RX state by means of an appropriate command.

Figure 5 illustrates the timing for this configuration. The rx_pkt_rvcd interrupt is not operational in this mode.

IEEE 802.15.4 Rx Symbol Clock SPORT Mode

The ADF7242 offers a symbol clock output option during IEEE802.15.4 packet reception. This option is useful when a tight timing synchronization between incoming packets and the network is required and the SFD interrupt (rx_sfd) cannot be used. The symbol clock output mode is enabled by setting gp_cfg.gpio_cfg=7 while the packet configuration is set to rc_cfg.rc_mode=0.

Interrupt Controller

CONFIGURATION REGISTERS

The integrated interrupt controller is capable of registering up to 16 different interrupt events. All interrupt events are registered in registers irq_src0 and irq_src1. The layout of both interrupt source registers is given in Table 18. An interrupt event sets the corresponding bit in register irq_src0 or irq_src1. The registers irq_src0 and irq_src1 may be read back to establish the source of an interrupt. A bit is reset by writing '1' to a particular bit location in register irq_src0 or irq_src1. If '0' is written to a bit location in the interrupt source registers, its state remains unchanged. This scheme facilitates hierarchical interrupt processing.

The interrupt mask registers irq1_en0, irq1_en1, irq2_en0 and irq2_en1 control which interrupt events are routed to one of the two interrupt pins IRQ1_GP1, and IRQ2_TRFS_GP2, respectively. If a bit in register irq1_en0, irq1_en1, irq2_en0 or irq2_en1 is set to '1', then the corresponding interrupt event can propagate to the IRQ1_GP1, or IRQ2_TRFS_GP2 pin. When not in SLEEP state, pins IRQ1_GP4 and IRQ2_TRFS_GP2 are configured as push-pull outputs, using positive logic polarity. When in SLEEP state, these pins have high impedance. The availability of two interrupt outputs permits a flexible allocation of interrupt source to two different MCU hardware resources. For instance, an rx_sfd interrupt may be associated with a timer-capture unit of the MCU, while all other interrupts are handled by a normal interrupt handling routine. When operating in SPORT mode, pin IRQ2_TRFS_GP2 acts as a frame synchronization signal and is disconnected from the interrupt controller.

Following a power-on reset or wake-up from SLEEP, the bits irq1_en0.powerup and irq2_en0.powerup are set, while all other bits in registers irq1_en0, irq1_en1, irq2_en0 and irq2_en1 are reset. Hence a powerup interrupt signal is asserted on pins IRQ1_GP4 and IRQ2_TRFS_GP2 after a power-on-reset event or wake-up from SLEEP state. Provided the wake-up from SLEEP event is caused by the wake-up timer, the powerup interrupt signal can hence be used to power up the user MCU.

Apart from the powerup interrupt, the rc_ready, wakeup and por interrupts are also asserted in the irq_src0 register. However, these interrupts are not propagated to the IRQ1_GP4 and IRQ2_TRFS_GP2 pins since the corresponding mask bits are reset. Registers irq_src0 and irq_src1 should be cleared during the initialization phase.

Table 17: Bit locations in registers irq_src0, irq1_en0, irq2_en0

Bit	Name	Notes
0	not in use	don't care; set mask to 0
1	powerup	Chip is ready for access
2	wakeup	Timer has timed out
3	rc_ready	Radio controller ready to accept new command
4	por	Power-On reset event
5	batt_alert	Battery voltage has dropped below programmed threshold value
6	not in use	don't care; set mask to 0
7	not in use	don't care; set mask to 0

Table 18: Bit locations in registers irq_src1, irq1_en1, irq2_en1

Bit	Name	Notes
0	cca_complete	CCA_RESULT in status word is valid
1	rx_sfd	SFD / sync word has been detected
2	tx_sfd	SFD / sync word has been transmitted
3	rx_pkt_rcvd	Packet received in RX_BUFFER
4	tx_pkt_sent	Tx packet transmission complete
5	not in use	don't care; set mask to 0
6	not in use	don't care; set mask to 0
7	not in use	don't care; set mask to 0

DESCRIPTION OF INTERRUPT SOURCES

cca_complete: Interrupt is asserted at the end of a CCA measurement following a RC_RX or RC_CCA command. The interrupt indicates that the CCA_RESULT flag in the status word is valid.

powerup: Interrupt is asserted if the ADF7242 is ready for SPI access following a wakeup from SLEEP state. This condition reflects a rising edge of the flag SPI_READY in the status word. If the ADF7242 has been woken up from SLEEP state using the CSN input this interrupt is useful to detect that the ADF7242 has powered up without the need to poll the SO output. The irq1_mask.powerup and the irq2_mask.powerup are automatically set on exit from SLEEP state. Hence this interrupt is generated whena transition from SLEEP is triggered by CSN being pulled low or by a timout event.

tx_pkt_sent: Interrupt is functional in IEEE 802.15.4 packet mode (rc_cfg.rc_mode=0) only. The interrupt is asserted when the transmission of an IEEE 802.15.4 packet in the TX_BUFFER is complete. Please refer to section IEEE 802.15.4 TX Packet Mode for details.

rx_pkt_received: Interrupt is functional in IEEE 802.15.4 packet mode (rc_cfg.rc_mode=0) only. The interrupt is asserted when an IEEE 802.15.4 packet has been received and is available in the RX_BUFFER. Please refer to section IEEE 802.15.4 RX Packet Mode for details.

wakeup: Interrupt is asserted if the WUC timer has decremented to zero. Prior to enabling this interrupt the WUC timer unit must be configured with registers tmr_cfg0, tmr_cfg1, tmr_rld0 and tmr_rld1. A wakeup interrupt may be

asserted while the ADF7242 is active, or has woken up from SLEEP state through a timeout event.

rx_sfd: Interrupt is asserted if a SFD or sync word is detected while in RX state. Please refer to sections IEEE802.15.4 Rx Timing and and GFSK/FSK Rx Timing and for details.

tx_sfd: Interrupt is asserted if the SFD is transmitted when IEEE 802.15.4 packet mode has been enabled (rc_cfg.rc_mode=0). Please refer to section IEEE802.15.4 Tx Timing and Control for details.

rc_ready: Interrupt is asserted if the radio controller is ready to accept a new command. This condition is equivalent to the rising edge of RC_READY flag in the status word.

batt_alert: Interrupt is asserted if the battery monitor signals a battery alarm. This occurs when the battery voltage drops below the programmed threshold value.The battery monitor must be enabled and configured.

WAKE UP CONTROLLER (WUC)

Circuit Description

The ADF7242 features a 16-bit wake-up timer with a programmable prescaler. The 32.768kHz RC oscillator or the 32.768kHz external crystal provides the clock source for the timer. This tick rate clocks a 3-bit programmable prescaler whose output clocks a pre-loadable 16-bit down-counter. An overview of the timer circuit is shown inFigure 43 . Table 19 lists the possible division rates for the prescaler. This combination of programmable prescaler and 16-bit down counter give a range a total WUC range of 30.52us to 36.4 hours.

The wake up interrupt can be enabled in register irq1_en0 or irq2_en0 to produce an interrupt when the timer has timed out.

Table 19. Prescaler Division Factors

wuc_config_high_wuc_prescaler (Location 0x30Ch)	32.768kHz Divider	Tick Period
000	1	30.52us
001	4	122.1us
010	8	244.1us
011	16	488.3us
100	128	3.91ms
101	1034	31.25ms
110	8192	250ms
111	65536	2000ms

Configuration and Operation

The wake up timer can be configured as follows:

- The clock signal for the timer is taken from the external 32.768 kHz crystal or the internal RC oscillator. This is selectable via tmr_cfg1.sleep_config.
- A 3-bit prescaler, which is programmable via tmr_cfg0.timer_prescal determines the tick period.
- This is followed by a preloadable 16 bit down counter. After the clock is selected, the reload value for the down counter (tmr_rld0 and tmr_rld1) and the prescaler values (tmr_cfg0.timer_prescal) may be programmed. Once the clock has been enabled, the counter will start to count down at the tick rate starting from the reload value. If wakeup interrupts are enabled the timer unit will generate an interrupt when the timer value reaches 0x0000. When armed, the wakeup interrupt will trigger a wake up from SLEEP.
- The reliable generation of wakeup interrupts requires the WUC time-out flag to be reset immediately after the reload value has been programmed as follows:

  Set configuration bit tmr_ctrl.wake_timer_flag_reset. Reset configuration bit tmr_ctrl.wake_timer_flag_reset.
- To enable automatic wake-up from SLEEP state arm the timer unit for wake up operation by setting configuration bit tmr_cfg1.wake_on_timeout. After writing this sequence to the ADF7242 a SLEEP command can be issued

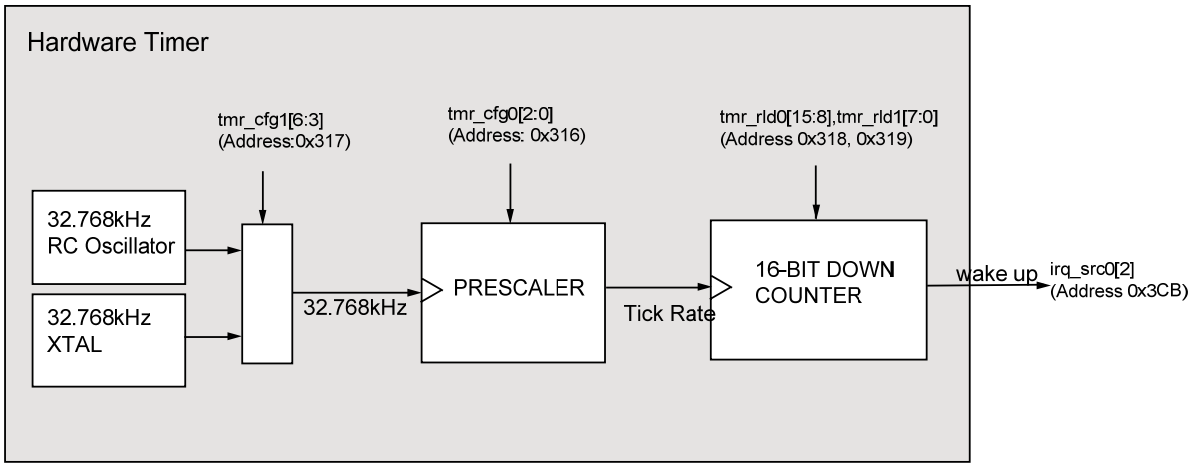


Figure 43. Hardware Wake up timer diagram

TABLE 20: REGISTER MAP OVERVIEW

Register Name	Address	Access Mode	Description
ext_ctrl	0x100	RW	External LNA/PA and internal PA control configuration bits
tx_fsk_test	0x101	RW	TX FSK test mode configuration
cca1	0x105	RW	RSSI threshold for CCA
cca2	0x106	RW	CCA mode configuration
buffercfg	0x107	RW	RX_BUFFER overwrite control
pkt_cfg	0x108	RW	FCS evaluation configuration
delaycfg0	0x109	RW	RC_RX command to SFD or sync word search delay
delaycfg1	0x10A	RW	RC_TX command to TX state
delaycfg2	0x10B	RW	Mac delay extention
sync_word0	0x10C	RW	sync word bits [7:0] of [23:0]
sync_word1	0x10D	RW	sync word bits [15:8] of [23:0]
sync_word2	0x10E	RW	sync word bits [23:16] of [23:0]
sync_config	0x10F	RW	sync word configuration
rc_cfg	0x13E	RW	RX / TX packet configuration
rc_var44	0x13F	RW	RESERVED
ch_freq0	0x300	RW	Channel Frequency Settings - Low Byte
ch_freq1	0x301	RW	Channel Frequency Settings - Middle Byte
ch_freq2	0x302	RW	Channel Frequency Settings - 2 MSBs
tx_fd	0x304	RW	TX Frequency Deviation Register
dm_cfg0	0x305	RW	RX Discriminator BW Register
tx_m	0x306	RW	TX Mode Register
rx_m	0x307	RW	RX Mode Register
rrb	0x30C	R	RSSI Readback Register
lrb	0x30D	R	Link Quality Readback Register
dr0	0x30E	RW	bits [15:8] of [15:0] for data rate setting
dr1	0x30F	RW	bits [7:0] of [15:0] for data rate setting

prampg	0x313	RW	RESERVED
txpb	0x314	RW	TX Packet Storage Base Address
rxpb	0x315	RW	RX Packet Storage Base Address
tmr_cfg0	0x316	RW	Wake up Timer Configuration Register - High Byte
tmr_cfg1	0x317	RW	Wake up Timer Configuration Register - Low Byte
tmr_rld0	0x318	RW	Wake up Timer Value Register - High Byte
tmr_rld1	0x319	RW	Wake up Timer Value Register - Low Byte
tmr_ctrl	0x31A	RW	Wake up Timer Timeout flag
pd_aux	0x31E	RW	Battmon enable
gp_cfg	0x32C	RW	GPIO Configuration
gp_out	0x32D	RW	GPIO Configuration
gp_in	0x32E	R	GPIO Configuration
synt	0x335	RW	bandwidth calibration timers
cal_cfg	0x33D	RW	Calibration Settings
synt_cal	0x371	RW	Oscillator and Doubler Configuration
iirf_cfg	0x389	RW	BB Filter Decimation Rate
cdr_cfg	0x38A	RW	CDR kVCO
dm_cfg1	0x38B	RW	Postdemodulator Filter
agcstat	0x38E	R	RXBB Ref Osc Calibration Engine Readback
rxcal0	0x395	RW	RX BB filter tuning, LSB
rxcal1	0x396	RW	RX BB filter tuning, MSB
rxfe_cfg	0x39B	RW	RXBB Ref Osc & RXFE Calibration
pa_rr	0x3A7	RW	Set PA ramp rate
pa_cfg	0x3A8	RW	PA enable
extpa_cfg	0x3A9	RW	External PA BIAS DAC
extpa_msc	0x3AA	RW	PA Bias Mode
adc_rbk	0x3AE	R	Readback temp
agc_cfg1	0x3B2	RW	GC Parameters

agc_max	0x3B4	RW	Slew rate
agc_cfg2	0x3B6	RW	RSSI Parameters
agc_cfg3	0x3B7	RW	RSSI Parameters
agc_cfg4	0x3B8	RW	RSSI Parameters
agc_cfg5	0x3B9	RW	RSSI & NDEC Parameters
agc_cfg6	0x3BA	RW	NDEC Parameters
ocl_cfg1	0x3C4	RW	OCL System Parameters
irq1_en0	0x3C7	RW	Interrupt Mask set bits [7:0] of [15:0] for IRQ1
irq1_en1	0x3C8	RW	Interrupt Mask set bits [15:8] of [15:0] for IRQ1
irq2_en0	0x3C9	RW	Interrupt Mask set bits [7:0] of [15:0] for IRQ2
irq2_en1	0x3CA	RW	Interrupt Mask set bits [15:8] of [15:0] for IRQ2
irq1_src0	0x3CB	RW	Interrupt Source bits [7:0] of [15:0] for IRQ
irq1_src1	0x3CC	RW	Interrupt Source bits [15:8] of [15:0] for IRQ
ocl_bw0	0x3D2	RW	OCL System Parameters
ocl_bw1	0x3D3	RW	OCL System Parameters
ocl_bw2	0x3D4	RW	OCL System Parameters
ocl_bw3	0x3D5	RW	OCL System Parameters
ocl_bw4	0x3D6	RW	OCL System Parameters
ocl_bws	0x3D7	RW	OCL System Parameters
ocl_cfg13	0x3E0	RW	OCL System Parameters
gp_drv	0x3E3	RW	I/O pads Configuration and bg trim
bm_cfg	0x3E6	RW	Battery Monitor Threshold Voltage setting
sfd_15_4	0x3F4	RW	Option to set non standard SFD
afc_cfg	0x3F7	RW	AFC mode and polarity
afc_ki_kp	0x3F8	RW	AFC ki and kp
afc_range	0x3F9	RW	AFC range
afc_read	0x3FA	RW	Readback frequency error

TABLE 21: REGISTER MAP DETAILS

Register address	Register name	Bit Field	Bit field Name	Access Mode	Reset Value	Description
0x100	ext_ctrl	[1:0]	RESERVED	RW	0	reserved, set to default
		[2]	extpa_auto_en	RW	0	1: RC enables external PA controller while in TX state, 0: pd_aux.extpa_bias_en is under user control
		[3]	txen_en	RW	0	1: TXEN_GP5 is set HI while in TX state and otherwise it is LO, 0: TXEN_GP5 is under user control – refer to register gp_out Refer to register gp_cfg for restrictions.
		[4]	rxen_en	RW	0	1: RXEN_GP6 is set HI while in RX state and otherwise it is LO, 0: RXEN_GP6 is under user control – refer to register gp_out Refer to register gp_cfg for restrictions.
		[7:5]	RESERVED	RW	0	reserved, set to default
0x101	tx_fsk_test	[0]	carrier_only	RW	0	Transmits unmodulated tone at the current Fch
		[1]	zero_one_pattern	RW	0	Transmit 0101 pattern
		[2]	zero_only	RW	0	Transmit one only (Fch+Fdev)
		[3]	one_only	RW	0	Transmit zero only (Fch-Fdev)
		[4]	pn16_only	RW	0	Transmit a Pseudo Random Binary Sequence
		[7:5]	RESERVED	RW	0	reserved, set to default
0x105	cca1	[7:0]	cca_thres	RW	171	RSSI threshold for CCA. Same scaling as rssi_readback. When CCA is completed: status word CCA_RESULT=1 if rrb.rssi_readback < cca.cca_thres; status word CCA_RESULT=0 if rrb.rssi_readback >= cca.cca_thres.
0x106	cca2	[0]	RESERVED	RW	0	reserved, set to default
		[1]	rx_auto_cca	RW	0	0 : Automatic CCA off 1 : Generate a CCA interrupt 128us after entering PHY_RX
		[2]	continuous_cca	RW	0	0 : Continuous CCA off 1 : Generate a CCA interrupt every 128us
		[7:3]	RESERVED	RW	0	reserved, set to default

0x107	buffercfg	[1:0]	rx_buffer_mode	RW	0	In IEEE 802.15.4 mode 0: First frame following RC_RX command is stored in RX_BUFFER. Device returns to PHY_RDY state after reception of first frame. 1: Continuous reception of frames enabled. New frame will overwrite previous frame. 2,3: reserved
		[2]	auto_rx_turnaround	RW	0	0: per rx_buffer_mode seting 1: Automaticaly goes to PHY_TX after RX packet received
		[3]	auto_tx_turnaround	RW	0	0: per tx_buffer_mode setting 1 : Automaticaly goes to PHY_RX after TX data transmitted
		[5:4]	tx_buffer_mode	RW	0	In IEEE 802.15.4 mode 0: Return to PHY_RDY after frame in TX_BUFFER is transmitted once. 1: Cyclic transmission of frame in TX_BUFFER after TX MAC delay with PA Rampup/down between packets 2: reserved 3: Cyclic transmission of frame in TX_BUFFER after TX MAC delay with PA kept on
		[6]	rand_tx_data	RW	0	0 : Transmit TX buffer data 1 : Transmit Random data
		[7]	trx_mac_delay	RW	0	0:tx_mac_delay enabled 1: tx _mac_delay diasabled
0x108	pkt_cfg	[0]	auto_fcs_off	RW	0	In IEEE 802.15.4 mode rx_pkt_received interrupt is asserted 0: Rx operation: FCS automatically validated. FCS replaced with RSSI and LQI values in RX_BUFFER Tx operation: FCS automatically appended to transmitted packet. FCS field in TX_BUFFER is ignored. 1: Rx operation: Received FCS is stored in RX_BUFFER without validation. Tx operation: FCS field in TX_BUFFER is transmitted.
		[3:2]	RESERVED	RW	0	reserved, set to default
		[4]	addon_en	RW	0	0: firmware addon module disabled 1: firmware addon module enabled. Module must have been loaded prior to setting this bit
		[7:5]	RESERVED	RW	0	reserved, set to default

0x109	delaycfg0	[7:0]	rx_mac_delay	RW	192	IEEE 802.15.4 mode: Programmable delay from issue of RC_RX command to SFD search and for start of RSSI measurement window. GFSK mode: Programmable delay from issue of RC_RX command to sync word search.
0x10A	delaycfg1	[7:0]	tx_mac_delay	RW	192	IEEE 802.15.4 mode & GFSK mode: Programmable delay from issue of RC_TX command to entering TX state
0x10B	delaycfg2	[7:0]	mac_delay_ext	RW	0	Programmable MAC delay extension
0x10C	sync_w0	[7:0]	sync_word[7:0]	RW	0	sync word bits [7:0] of [23:0]
0x10D	sync_w1	[7:0]	sync_word[15:8]	RW	0	sync word bits [15:8] of [23:0]
0x10E	sync_w2	[7:0]	sync_word[23:16]	RW	0	sync word bits [23:16] of [23:0]
0x10F	sync_cfg	[4:0]	sync_len	RW	0	Synchronization word length which may be from 0 to 24. 0: sync word detection disabled. 25..31: reserved
		[6:5]	sync_tol	RW	0	Number of bit mismatches allowed: 0 to 3 4..7: reserved
		[7]	RESERVED	RW	0	reserved, set to default
0x13E	rc_cfg	[7:0]	rc_mode	RW	0	Configure packet format: 0: IEEE 802.15.4 packet mode 1: reserved 2: IEEE 802.15.4 continuous mode 3: FSK streaming mode 4..255: reserved
0x13F	rc_var44	[7:0]	RESERVED	RW	0	reserved, do not access
0x300	ch_freq0	[7:0]	ch_freq[7:0]	RW	128	(channel frequency [Hz] / 10kHz), bits [7:0] of [23:0]
0x301	ch_freq1	[7:0]	ch_freq[15:8]	RW	169	(channel frequency [Hz] / 10kHz) bits [15:8] of [23:0];
0x302	ch_freq2	[7:0]	ch_freq[23:16]	RW	3	(channel frequency [Hz] / 10kHz) bits [23:16] of [23:0];

0x304	tx_fd	[5:0]	tx_freq_dev	RW	50	TX frequency deviation =tx_freq_dev * 10 kHz Recommendations settings: 62.5kbps..125kbps: 6 250kbps: 13 500kbps: 13 1000kbps: 25 2000kbps: 50
		[7:6]	RESERVED	RW	0	reserved, set to default
0x305	dm_cfg0	[3:0]	discriminator_bw	RW	6	RX discriminator bandwidth. Set to 3.25MHz/(rx frequency deviation). Recommendations settings: 62.5kbps..125kbps: 54 250kbps: 25 500kbps: 25 1000kbps: 13 2000kbps: 6
		[7:4]	RESERVED	RW	0	reserved, set to default
0x306	tx_m	[0]	preemp_filt	RW	0	1: enable, 0: disable preemphasis filter. Set for data rate > 250kbps and IEEE 802.15.4
		[1]	gauss_filt	RW	0	1: GFSK, 0: FSK
		[4:2]	tx_modulation	RW	0	1 : GFSK/FSK 5 : IEEE 802.15.4 2, 3, 5..7: reserved
		[7:5]	RC_CONTROLLED	RW	0	Controlled by radio controller
0x307	rx_m	[1:0]	RESERVED	RW	0	reserved, set to default
		[4:2]	rx_modulation	RW	0	1 : GFSK/FSK 4 : IEEE 802.15.4 0, 2, 3, 5..7: reserved
		[5]	RESERVED	RW	0	reserved, set to default
		[7:6]	RC_CONTROLLED	RW	0	Controlled by radio controller
0x30C	rrb	[7:0]	rssi_readback	R	0	RX input power in dBm; signed 2s-complement
0x30D	lrb	[7:0]	lqi_readback	R	0	Link Quality Readback Value
0x30E	dr0	[7:0]	data_rate_high	RW	78	data rate: 256 * data_rate_high *100bits/s +dr1
0x30F	dr1	[7:0]	data_rate_low	RW	32	data rate: data_rate_low *100bits/s +dr0
0x313	prampg	[3:0]	pram_page	RW	0	reserved, set to default

		[7:4]	RESERVED	RW	0	reserved, set to default
0x314	txpb	[7:0]	tx_pkt_base	RW	128	Base address of TX_BUFFER in packet RAM
0x315	rxpb	[7:0]	rx_pkt_base	RW	0	Base address of RX_BUFFER in packet RAM
0x316	tmr_cfg0	[2:0]	timer_prescal	W	0	Divider factor for XTO32K or RCO 0: ÷1 1: ÷4 2: ÷8 3: ÷16 4: ÷128 5: ÷1024 6: ÷8192 7: ÷65536 Note that this is a write only register and should be written to prior to writing to register tmr_cfg1. Settings become effective only after writing to register tmr_cfg1.
		[7:3]	RESERVED	W	0	reserved, set to default
0x317	tmr_cfg1	[0]	wake_on_timeout	W	0	1: enable, 0:disable wake-up on time-out event
		[2:1]	RESERVED	W	0	reserved, set to default
		[6:3]	sleep_config	W	0	0: SLEEP_DEEP 1: SLEEP_BBRAM 4: SLEEP_XTO 5: SLEEP_BBRAM_XTO 11: SLEEP_BBRAM_RCO 3,6..10,12..15: reserved Refer to note in register tmr_cfg0.
		[7]	RESERVED	W	0	reserved, set to default
0x318	tmr_rld0	[7:0]	timer_reload[15:8]	W	0	timer reload value, bits [15:8] of [15:0] Note that this is a write only register and should be written to prior to writing to register tmr_rld1. Settings become effective only after writing to register tmr_rld1.
0x319	tmr_rld1	[7:0]	timer_reload[7:0]	W	0	timer reload value, bits [7:0] of [15:0] Refer to note in register tmr_rld0
0x31A	tmr_ctrl	[0]	wake_timer_flag_reset	W	0	timer flaf reset
		[[6:0]	RESERVED	W	0	reserved, set to default
0x31E	pd_aux	[0]	RC_CONTROLLED	RW	0	Controlled by radio controller
		[1]	RC_CONTROLLED	RW	0	Controlled by radio controller

		[2]	RC_CONTROLLED	RW	0	Controlled by radio controller
		[3]	RC_CONTROLLED	RW	0	Controlled by radio controller
		[4]	extpa_bias_en	RW	0	1: enable, 0: disable external PA biasing circuit. Controlled by radio controller when ext_ctrl.extpa_rc_ctrl_en =1
		[5]	battmon_en	RW	0	1: enable, 0: disable battery monitor;
		[6]	RC_CONTROLLED	RW	0	Controlled by radio controller
		[7]	RESERVED	RW	0	reserved, set to default.
0x32C	gp_cfg	[7:0]	gpio_config	RW	0	0: IRQ1, IRQ2 functionality gp_out.gpio_dout[6] controls RXEN output gp_out.gpio_dout[5] controls TXEN output 1..3: reserved 4[1]: GP[7:0] are outputs of gp_out.gpio_dout[7:0] 5[1]: GP[7:0] are inputs to gp_in.gpio_din[7:0] 6: IRQ1 , DR, DT, TRFS, TRCLK functionality gp_out.gpio_dout[6] controls RXEN output gp_out.gpio_dout[5] controls TXEN output 103: IRQ1 , DR, DT, IRQ2, TRCLK functionality gp_out.gpio_dout[6] controls RXEN output gp_out.gpio_dout[5] controls TXEN output 7:102,104:255 reserved [1] precludes 32kHz xtal oscillator operation
0x32D	gp_out	[7:0]	gpio_dout	RW	0	GPIO output value if gp_cfg.gpio_config = 4 gp_out.gpio_dout[7:0] -> GP[7:0] If ext_ctrl.rxen_en= 1 then gp_out.gpio_dout[6] is controlled by radio controller. If ext_ctrl.txen_en= 1 then gp_out.gpio_dout[5] is controlled by radio controller
0x32E	gp_in	[7:0]	gpio_din	R	0	GPIO readback value if gp_cfg.gpio_config = 5 GP[7:0] -> gp_in.gpio_din[7:0]
0x335	synt	[7,0]	lock_time	RW	10	Synthesiser locking timeout period
0x33D	cal_cfg	[1:0]	skip_rc_vco_cal	RW	0	0: do not skip VCO and RC calibration. This calibration is only required when changing channels or going from IDLE to PHY_RDY or IDLE to RX. 3: skip VCO and RC calibration.
		[3:2]	skip_tx_cal	RW	0	0: do not skip modulation bandwidth calibration on transition into PHY_RDY state 3: skip modulation bandwidth calibration on transition into PHY_RDY state. Use when data rate < =250kbps. 1,2: reserved

		[7:4]	RESERVED	RW	3	Reserved, set to default
0x36E	vco_cal	[0]	synt_qtune_ovrw_en	RW	1	Set to default
		[6:1]	synt_qtune_ovrw_val	RW	50	IEEE 802.15.4:per default GFSK: set to 55
0x371	synt_cal	[2:0]	RESERVED	RW	0	reserved, set to default
		[5:3]	xto26_trim	RW	4.	26MHz crystal oscillator (XOSC26N) tuning capacitor control word The load capacitance is adjusted according to the value of xto26_trim as follows: 0: -4*187.5fF 1: -3*187.5fF 2: -2*187.5fF 3: -1*187.5fF 4: 0*187.5fF 5: 1*187.5fF 6: 2*187.5fF 7: 3*187.5fF
		[7:6]	RESERVED	RW	0	reserved, set to default
0x389	iirf_cfg	[1:0]	iir_stage1_bw	RW	1	RX baseband digital filter stage 1 sampling rate fs1=13MHz/(2^ iir_stage1_bw). IEEE 802.15.4: set to default GFSK 62.5kbps..1000kbps: 2 2000kbps: 1
		[4:2]	iir_stage2_bw	RW	1	RX baseband digital filter stage 2 sampling rate fs2=fs1/(2^ iir_stage2_bw). IEEE 802.15.4: per default GFSK 62.5kbps..250kbps: 4 500kbps: 3 1000kbps: 2 2000kbps: 1
		[7:5]	RESERVED	RW	0	reserved, set to default
0x38A	cdr_cfg	[3:0]	cdr_kvco	RW	0	IEEE 802.15.4 mode: per default GFSK mode: 62.5kbps:2, 125kbps :2, 250kbps:0, 500kbps: 0, 1000kbps: 0, 2000: 0
		[7:4]	RESERVED	RW	15	reserved, set to default

0x38B	dm_cfg1	[7:0]	postdemod_bw	RW	128	Post demodulator filter BW= postdemod_bw*15kHz IEEE 802.15.4: 133; GFSK 62.5kbsp: 4, 125kbps:8, 250kbps:17, 500kbps:33, 1000kbps:67, 2000kbps:133
0x38E	agcstat	[5:0]	RESERVED	R	0	reserved, set to default
		[6]	agc_settled	R	0	RX-path AGC 1: has settled, 0: is in transient state
		[7]	RESERVED	R	0	ignore
0x395	rxcal0	[7:0]	dcap_ovwrt _low	RW	0	RXBB filter tuning overwrite word, LSB
0x396	rxcal1	[0]	dcap_ovwrt _high	RW	0	RXBB filter tuning overwrite word, MSB
		[1]	dcap_ovwrt_en	RW	0	RXBB filter tuning overwrite word enable
		[7:2]	RESERVED	RW	2	reserved, set to default
0x39B	rxfe_cfg	[3:0]	rxbb_bw_ana	RW	13	RXBB analogue filter bandwidth= rxbb_bw_ana *100kHz (minimum 600kHz) IEEE 802.15.4 mode: per default GFSK 62.5kbps..1000kbps: 6 2000kbps: 11
		[6:4]	lna_sel	RW	0	RX front end state machine LNA configuration: 0: LNA1 1: LNA2 7..2 : reserved
		[7]	RESERVED	RW	0	reserved, set to default
0x3A7	pa_rr	[2:0]	pa_ramp_rate	RW	0	PA ramp rate: (2^(pa_rr.pa_ramp_rate)*2.4ns per PA power step
		[6:3]	RESERVED	RW	0	Default 0. Set to default
		[7]	RESERVED	RW	0	reserved, set to default
0x3A8	pa_cfg	[4:0]	pa_bridge_dbias	RW	21	Controlled by radio controller in final silicon.
		[6:5]	pa_controller_en	RW	2	PA configuration during TX state: 0: PA controller disabled 2: PA controller enabled 1,3: reserved
		[7]	RESERVED	RW	0	reserved, set to default

0x3A9	extpa_cfg	[4:0]	extpa_bias	RW	0	If extpa_msc.extpa_bias_mode = {1, 2, 3, or 4}: PABIOP pin DAC current equals 80uA - 2.58 uA * extpa_bias. If extpa_msc.extpa_bias_mode={5 or 6}: PAVSUP pin servo current set point equal 25mA - 0.8064mA * extpa_bias
		[7:5]	RESERVED	RW	0	reserved, set to default
0x3AA	extpa_msc	[2:0]	extpa_bias_mode	RW	1	External PA interface configuration: 0: PA_VSUP: on; PA_BIASOP: floating 1: PA_VSUP: on; PA_BIASOP: I source 2: PA_VSUP: on; PA_BIASOP: I sink 3: PA_VSUP: off; PA_BIASOP: I source 4: PA_VSUP: off; PA_BIASOP: I sink 5: PA_VSUP: on; PA_BIASOP: pos servo o/p 6: PA_VSUP: on; PA_BIASOP: neg servo o/p 7: reserved
		[3]	extpa_bias_src	RW	0	0: select Rbias- referred reference current 1: select bandgap- referred reference current
		[7:4]	pa_pwr	RW	15	PA output power after ramping phase: 0: min power 15: max power Nominal power step size 2dB per LSB
0x3AB	pa_bias1	[5:0]	pa_pt_bias	RW	11	IEEE 802.15.4: set to 10 GFSK: 125kbps: set to 10 2Mbps: set to 9
		[7:6]	RESERVED	RW	0	reserved, set to default
0x3AC	pa_bias2	[5:0]	pa_vgb_bias	RW	11	IEEE 802.15.4: set to 10 GFSK: 125kbps: set to 10 2Mbps: set to 9
		[7:6]	RESERVED	RW	0	reserved, set to default
0x3AE	adc_rbk	[5:0]	adc_out	R	0	ADC output code
		[7:6]	RESERVED	R	0	ignore
0x3B2	agc_cfg1	[0]	agc_lock	RW	0	0: enable, 1: freeze AGC
		[4:1]	agc_lna_thres	RW	16	Sets number of PGA attenuation steps prior to first LNA attenuation step.
		[6:5]	agc_lna_hyst	RW	1	Hysteresis in terms of PGA attenuation steps for LNA gain transitions

		[7]	RESERVED	RW	0	reserved, set to default
0x3B4	agc_max	[2:0]	RESERVED	RW	0	reserved, set to default
		[5:3]	agc_sat_thres_offs	RW	2	ADC saturation detection threshold offset from fullscale. The AGC enters slewing mode when this threshold is exceeded.
		[7:6]	RESERVED	RW	2	reserved, set to default
0x3B6	agc_cfg2	[6:0]	agc_thres_hi	RW	36	AGC upper RSSI trigger threshold IEEE 802.15.4 set to default GFSK mode set to 55
		[7]	RESERVED	RW	0	reserved, set to default
0x3B7	agc_cfg3	[6:0]	agc_target	RW	25	AGC RSSI active state target value IEEE 802.15.4 set to default GFSK mode set to 42
		[7]	RESERVED	RW	0	reserved, set to default
0x3B8	agc_cfg4	[6:0]	agc_thres_lo	RW	14	AGC lower RSSI trigger threshold IEEE 802.15.4 set to default GFSK mode set to 30
		[7]	RESERVED	RW	0	reserved, set to default
0x3B9	agc_cfg5	[1:0]	rssi_avg_time	RW	2	RSSI averaging time . Default per IEEE802.15.4. Refer datasheet RSSI section for further details.
		[4:2]	rssi_offs	RW	4	RSSI offset adjust, rssi_offs is added to rrb.rssi_readback
		[7:5]	agc_filt1_tavg	RW	0	AGC prefilter averaging time. IEEE802.15.4 set to default. For GFSK data rate(kbps): 62.5:0; 125:0; 250:0; 500:0; 1000:0; 2000:0
0x3BA	agc_cfg6	[2:0]	agc_filt2_tavg1	RW	6	AGC post filter averaging time for LNA transition. IEEE802.15.4 per default. For GFSK/FSK per default
		[5:3]	agc_filt2_tavg2	RW	6	AGC post filter averaging time.IEEE802.15.4 per default. For GFSK per default
		[7;6]	RESERVED	RW	0	reserved, set to default
0x3C4	ocl_ cfg1	[7:0]	ocl_fsk_lock_timeout	RW	3	IEEE802.15.4 per default. For GFSK/FSK set to 12
0x3C7	irq1_en0	[0]	Reserved	RW1	0	set to 0
		[1]	powerup	RW1	0	Chip is ready for access
		[2]	wakeup	RW1	0	Timer has timed out

		[3]	rc_ready	RW1	0	Radio controller ready to accept new command
		[4]	por	RW1	0	Power-On reset event
		[5]	batt_alert	RW1	0	Battery monitor interrupt
		[6]	Reserved	RW1	0	set to 0
		[7]	Reserved	RW1	0	set to 0
0x3C8	irq1_en1	[0]	cca_complete	RW1	0	CCA_RESULT in status word is valid
		[1]	rx_sfd	RW1	0	SFD / sync word has been detected
		[2]	tx_sfd	RW1	0	SFD / sync word has been transmitted
		[3]	rx_pkt_rcvd	RW1	0	Packet received in RX_BUFFER
		[4]	tx_pkt_sent	RW1	0	Tx packet transmission complete
		[5]	Reserved	RW1	0	set to 0
		[6]	Reserved	RW1	0	set to 0
		[7]	Reserved	RW1	0	set to 0
0x3C9	irq2_en0	[0]	Reserved	RW1	0	set to 0
		[1]	powerup	RW1	0	Chip is ready for access
		[2]	wakeup	RW1	0	Timer has timed out
		[3]	rc_ready	RW1	0	Radio controller ready to accept new command
		[4]	por	RW1	0	Power-On reset event
		[5]	batt_alert	RW1	0	Battery monitor interrupt
		[6]	Reserved	RW1	0	set to 0
		[7]	Reserved	RW1	0	set to 0
0x3CA	irq2_en1	[0]	cca_complete	RW1	0	CCA_RESULT in status word is valid
		[1]	rx_sfd	RW1	0	SFD / sync word has been detected
		[2]	tx_sfd	RW1	0	SFD / sync word has been transmitted
		[3]	rx_pkt_rcvd	RW1	0	Packet received in RX_BUFFER
		[4]	tx_pkt_sent	RW1	0	Tx packet transmission complete
		[5]	Reserved	RW1	0	set to 0
		[6]	Reserved	RW1	0	set to 0
		[7]	Reserved	RW1	0	set to 0

0x3CB	irq_src0	[0]	Reserved	RW1	0	set to 0
		[1]	powerup	RW1	0	Chip is ready for access
		[2]	wakeup	RW1	0	Timer has timed out
		[3]	rc_ready	RW1	0	Radio controller ready to accept new command
		[4]	por	RW1	0	Power-On reset event
		[5]	batt_alert	RW1	0	Battery monitor interrupt
		[6]	Reserved	RW1	0	set to 0
		[7]	Reserved	RW1	0	set to 0
0x3CC	irq_src1	[0]	cca_complete	RW1	0	CCA_RESULT in status word is valid
		[1]	rx_sfd	RW1	0	SFD / sync word has been detected
		[2]	tx_sfd	RW1	0	SFD / sync word has been transmitted
		[3]	rx_pkt_rcvd	RW1	0	Packet received in RX_BUFFER
		[4]	tx_pkt_sent	RW1	0	Tx packet transmission complete
		[5]	Reserved	RW1	0	set to 0
		[6]	Reserved	RW1	0	set to 0
		[7]	Reserved	RW1	0	set to 0
0x3D2	ocl_bw0	[4:0]	ocl_bw0	RW	27	For IEEE 802.15.4 set to default. For GFSK/FSK set to 27
		[7:5]	RESERVED	RW	0	reserved, set to default
0x3D3	ocl_bw1	[4:0]	ocl_bw1	RW	26	For IEEE 802.15.4 set to default. For GFSK/FSK set to 26
		[7:5]	RESERVED	RW	0	reserved, set to default
0x3D4	ocl_bw2	[4:0]	ocl_bw2	RW	2	For IEEE 802.15.4 set to default. For GFSK/FSK set to 30
		[7:5]	RESERVED	RW	0	reserved, set to default
0x3D5	ocl_bw3	[4:0]	ocl_bw3	RW	3	For IEEE 802.15.4 set to default. For GFSK/FSK set to 30
		[7:5]	RESERVED	RW	0	reserved, set to default
0x3D6	ocl_bw4	[4:0]	ocl_bw4	RW	2	For IEEE 802.15.4 set to default. For GFSK/FSK set to 30

		[7:5]	RESERVED	RW	0	reserved, set to default
0x3D7	ocl_bws	[4:0]	ocl_bw	RW	29	For IEEE 802.15.4 set to default. For GFSK set to 30
		[7:5]	RESERVED	RW	0	reserved, set to default
0x3E0	ocl_cfg13	[0]	RESERVED	RW	0	reserved, set to default
		[1]	ocl_sosi_en	RW	1	For IEEE 802.15.4 set to default. For GFSK set to 0
		[7:2]	RESERVED	RW	60	reserved, set to default
0x3E3	gp_drv	[1:0]	gpio_drive	RW	0	GPIO + SPI drive strength; 0: 4mA; 1:8mA; 2: >8mA; 3: reserved
		[3:2]	gpio_slew	RW	0	GPIO + SPI slew rate; 0: very slow; 1: slow; 2: very fast; 3: fast
		[7:4]	RESERVED	RW	0	reserved, set to default
0x3E6	bm_cfg	[4:0]	battmon_voltage	RW	0	Battery monitor trip voltage: 1.7V + 62mV * battmon_voltage; batt_alert interrupt is asserted when V_{DDBAT} drops below the trip voltage.
0x3F4	sfd_15_4	[3:0]	sfd_symbol_1	RW	7	symbol1 of SFD Note: 802.15.4 requires SFD1 = 7
		[7:4]	sfd_symbol_2	RW	10	symbol 2 of SFD Note: 802.15.4 requires SFD1 = 10
0x3F7	afc_cfg	[1:0]	afc_mode	RW	0	sets AFC mode
		[2]	afc_polarity	RW	0	set AFC polarity
		[7:3]	RESERVED	RW	0	reserved, set to default
0x3F8	afc_ki_kp	[3:0]	afc_ki	RW	0	Sets the AFC PI controller proportional gain. For IEEE 802.15.4 not used. For GFSK data rate(kbps): 62.5:10; 125:10; 250:9; 500:9; 1000:9; 2000:9
		[7:4]	afc_kp	RW	0	Sets the AFC PI controller integral gain. For IEEE 802.15.4 not used. For GFSK data rate(kbps): 62.5:7; 125:7; 250:7; 500:7; 1000:7; 2000:9
0x3F9	afc_range	[7:0]	max_afc_range	RW	0	Limits the AFC pull-in Range. Should be set to half the receive baseband filter bandwidth. AFC pull in range is ±max_afc_range kHz
0x3FA	afc_read	[7:0]	afc_freq_error	RW	0	Frequency error read back. Error: 1kHz/lsb

APPLICATIONS CIRCUITS

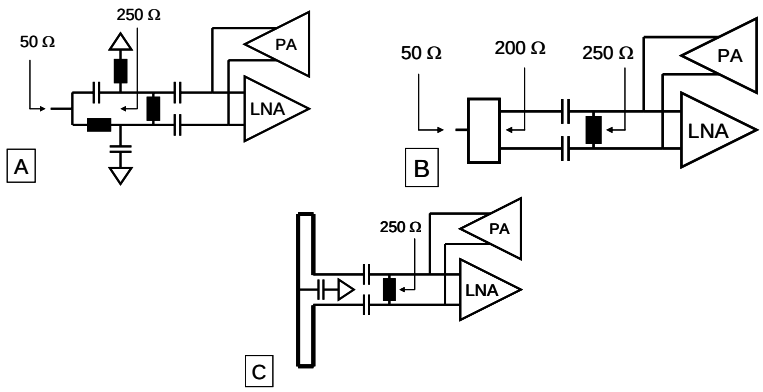


Figure 44.RF balun/antenna configurations (A: discrete; B: dielectric balun; C: dipole antenna)

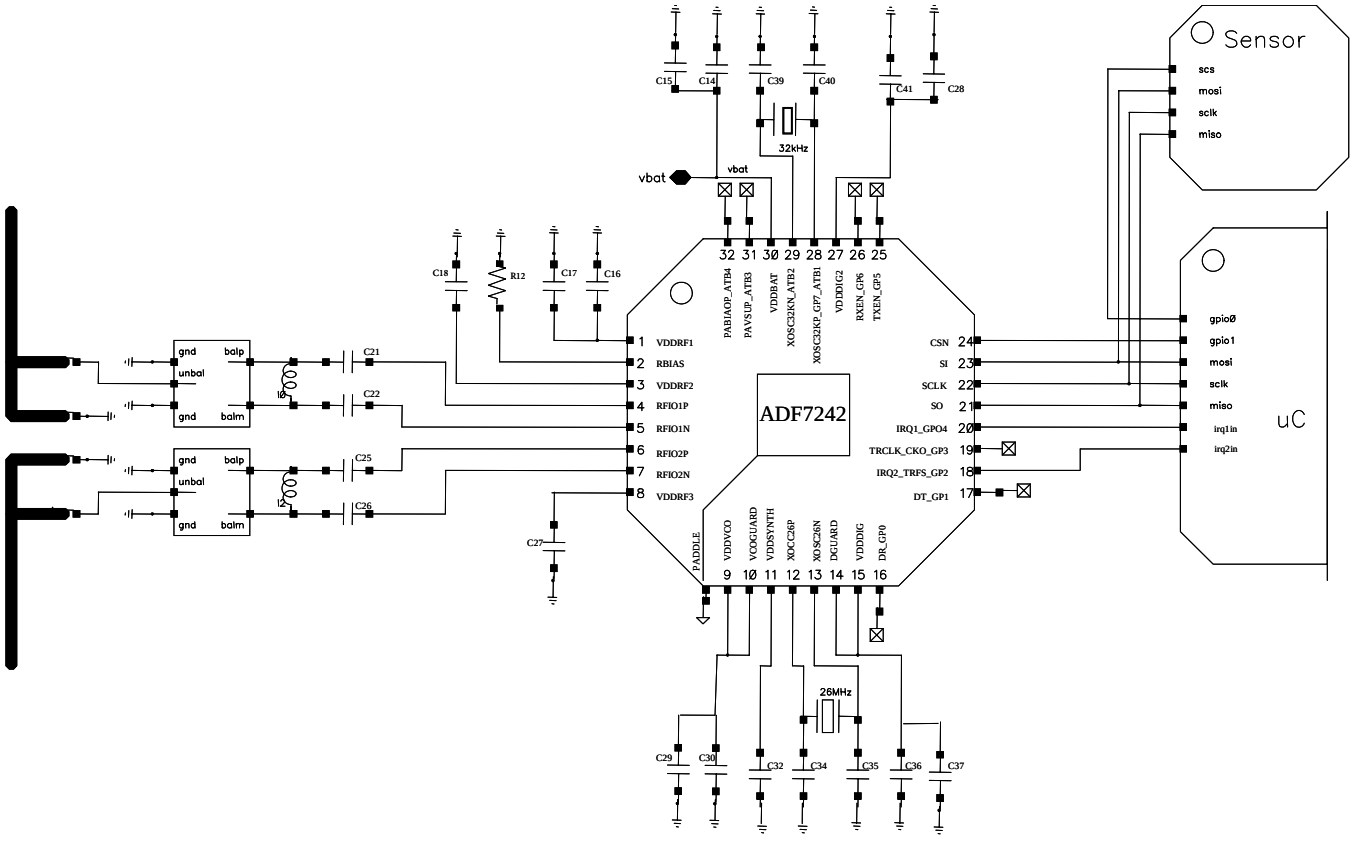


Figure 45.Typical ADF7242 application circuit using antenna diversity

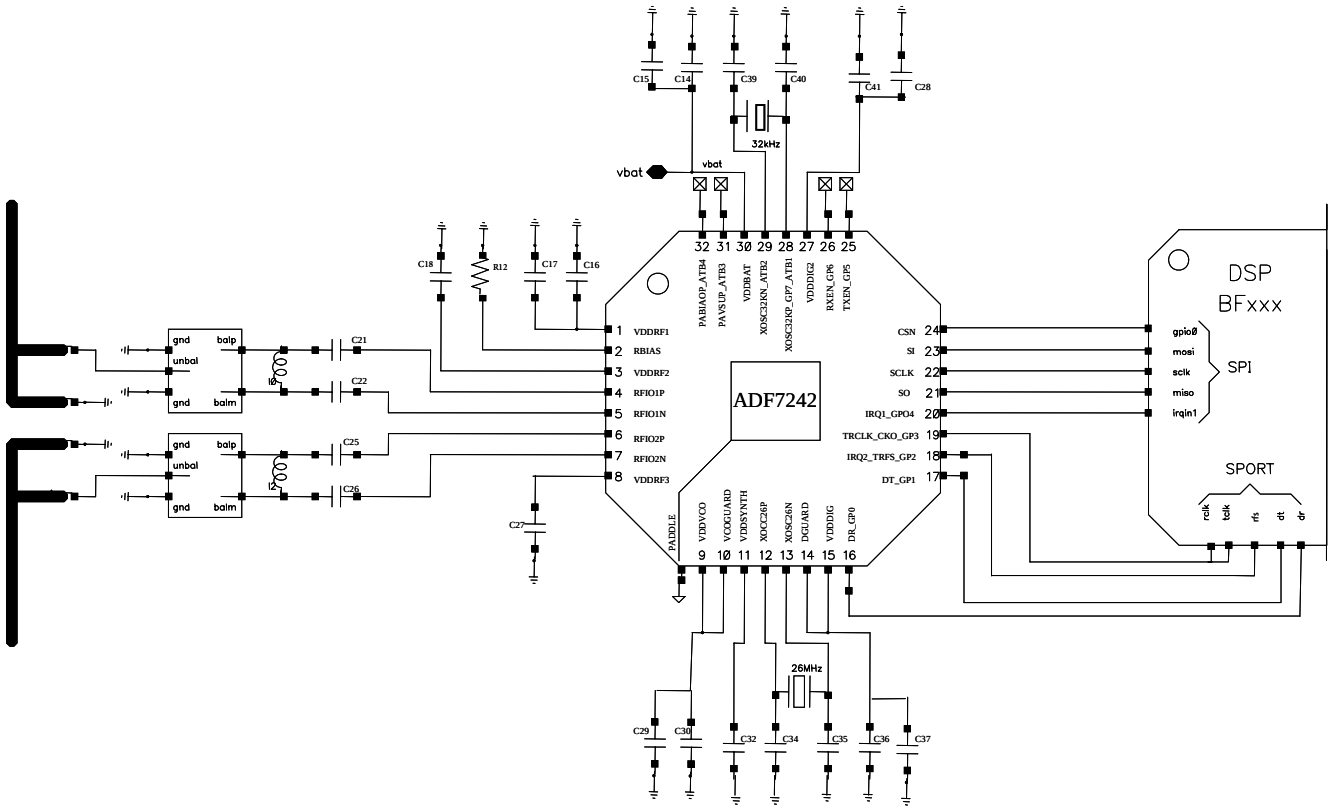
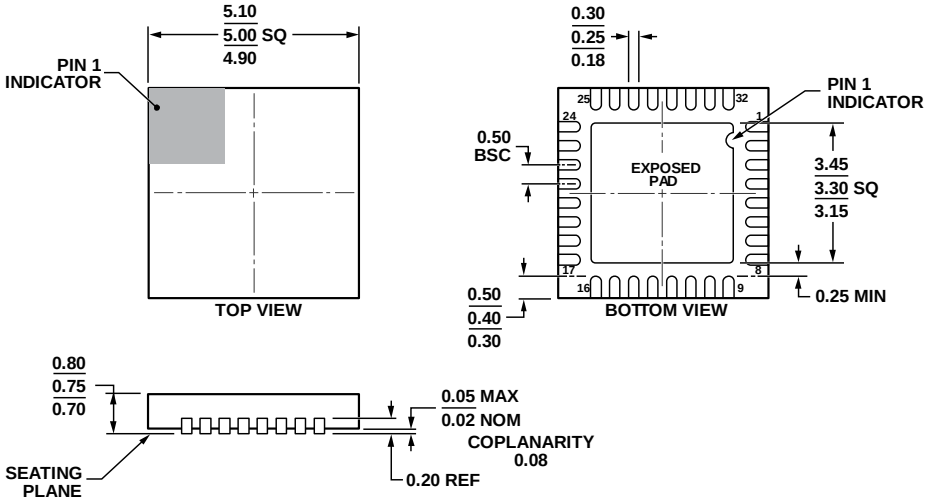


Figure 46.Typical ADF7242 application circuit with DSP using antenna diversity

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARD MO-220-VHHD-2

Figure 47. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 x 5 mm Body, Very Thin Quad (CP-32-13)
Dimensions shown in millimeters

PR08912-0-3/10(PrG)